

Starlord KBL Refresh Schematics KabyLake-R

2017-05-25

REV : A00


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DY : None Installed

UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Core Design>

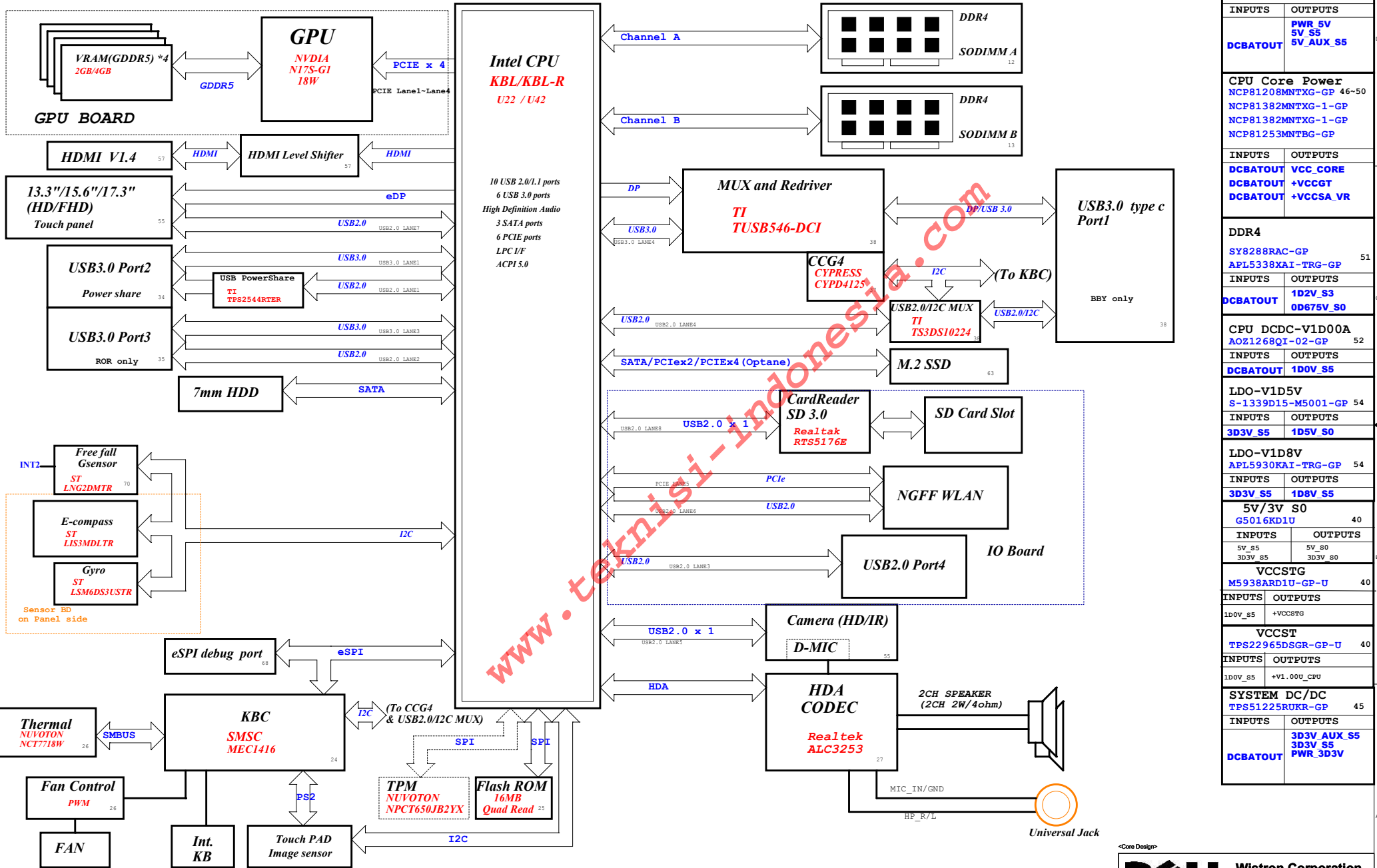
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Title			
Cover Page			
Size A3	Document Number		Rev A00
Date: Monday, August 28, 2017	Sheet	1	of 106

Project code: 4PD0CF010001(SL13_R)
4PD0CG010001(SL15_R)
4PD0CH010001(SL17_B)

PCB P/N: 16888
Revision: A00

Star lord KBL Block Diagram

	SENSOR	IO	MB
ROR	17A18-SA	17A17-SA	17810-1
BBY	17A18-SA	17A16-SA	16888-1




CHARGER		44
ISL88739		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		45
SY8288CRAC-GP		
INPUTS	OUTPUTS	
DCBATOUT	PWR 5V 5V_S5 5V_AUX_S5	
CPU Core Power		46-50
NCP81208MNTXG-GP		
NCP81382MNTXG-1-GP		
NCP81382MNTXG-1-GP		
NCP81253MNTBG-GP		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DCBATOUT	+VCCGT	
DCBATOUT	+VCCSA_VR	
DDR4		51
SY8288RAC-GP		
APL5338KAI-TRG-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3 0D675V_S0	
CPU DCDC-V1D00A		52
AOZ1268Q1-02-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	
LDO-V1D5V		54
S-1339D15-M5001-GP		
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
LDO-V1D8V		54
APL5930KAI-TRG-GP		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
5V/3V S0		40
G5016KD1U		
INPUTS	OUTPUTS	
5V_S5 3D3V_S5	5V_S0 3D3V_S0	
VCCSTG		40
M5938ARD1U-GP-U		
INPUTS	OUTPUTS	
1D0V_S5	+VCCSTG	
VCCST		40
TPS22965DSGR-GP-U		
INPUTS	OUTPUTS	
1D0V_S5	+V1.00V_CPU	
SYSTEM DC/DC		45
TPS51225RUKR-GP		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 3D3V_S5 PWR_3D3V	

SSID = CPU

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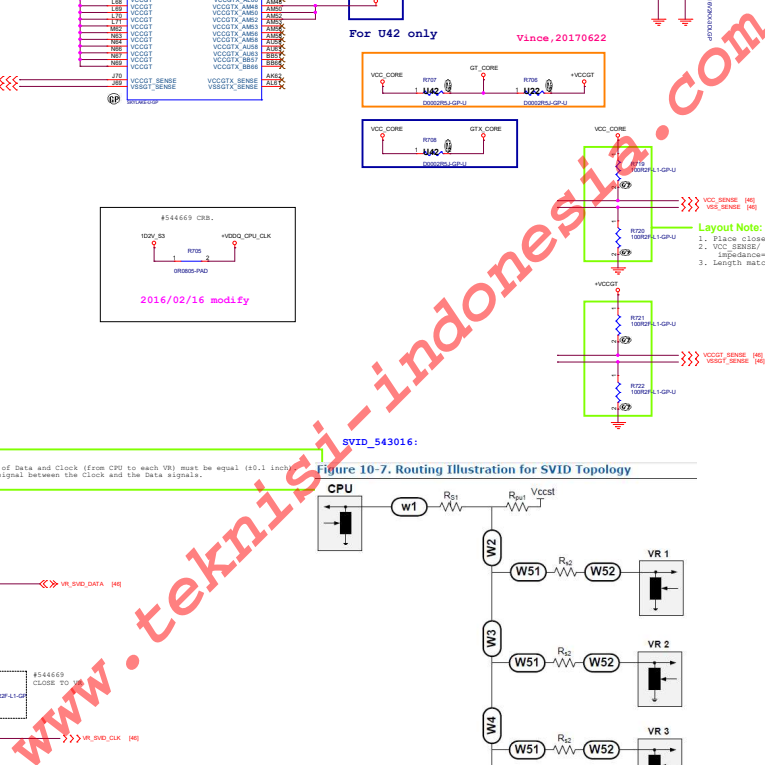
Starlord KBL-R

Rev

A00

Date: Monday, August 28, 2017

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SVID CLOCK

Layout Note:
The total Length
Route the Aircraft

Layout Note:
The total Length
Route the Aircraft

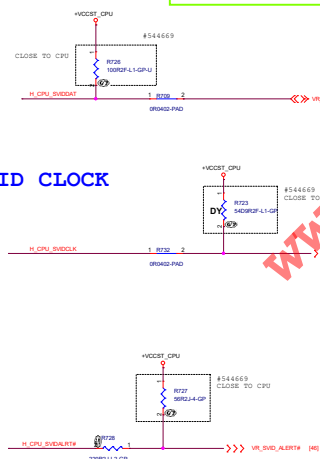


Figure 10-7. Routing Illustration for SVID Topology

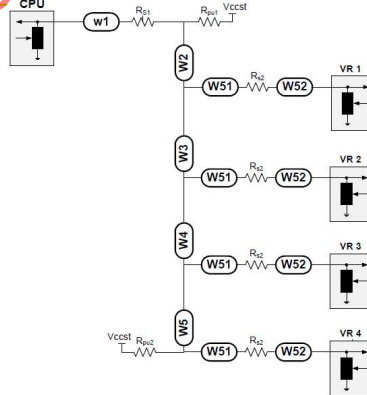
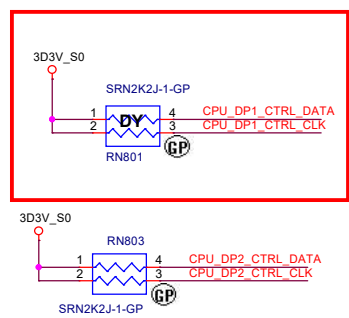


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R _{RD1} [2]	R _{RD2} [2]	R ₃ [2]	R ₅₂ [2]	VCC [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSKC							Empty	45	0	50	
VIDALERT #							56	Empt Y	220	0	

Dummy, Vendor suggest
20141117

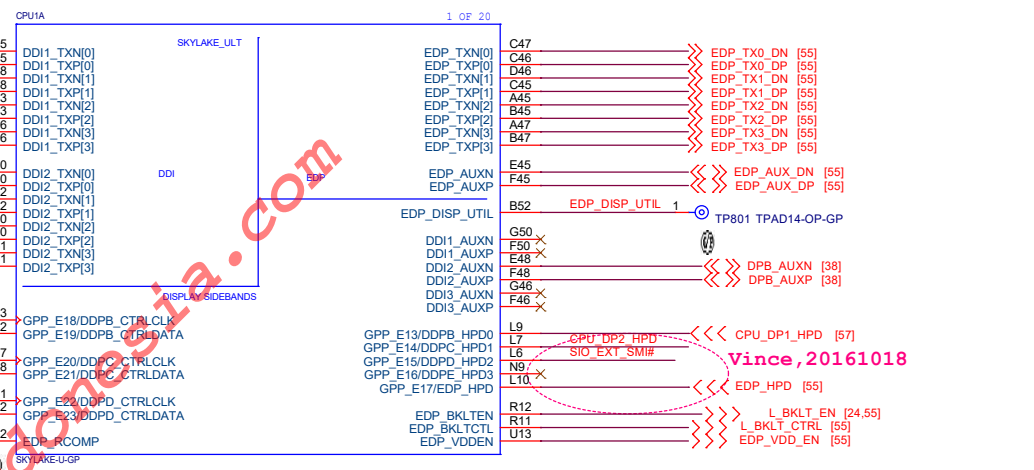
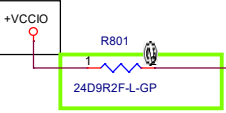


HDMI

DP and DP to VGA

HDMI

Check



(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

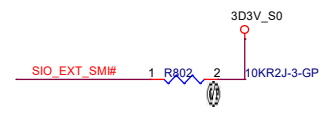
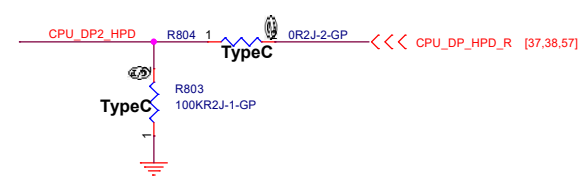
(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 Ω resistor.




Main Func = CPU

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(#543016 PDS)

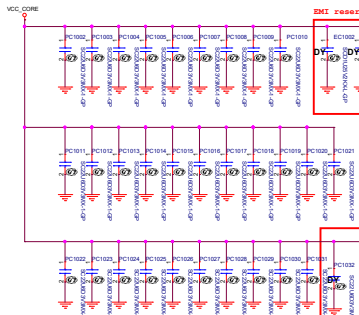
Vince, 20160922

CORE

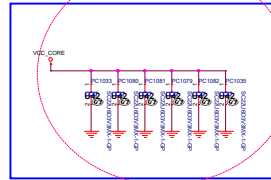
20140814 DAVID

U-line 23e 28W
IocMax current-I0ma max = 34 A
220 0603 x 35(5 DV)

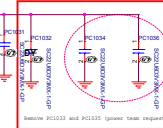
DMI 6888V6 , 20141118



For U42

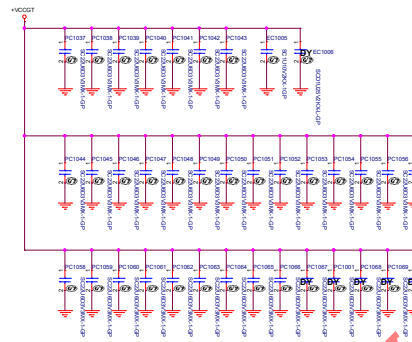


Vince, 20161005



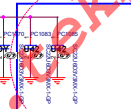
SLICED GT

U-line 23e 28W
IocMax current-I0ma max[A] = 67 A
220 0603 x35 (5 DV)



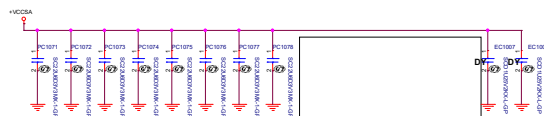
U42

Vince, 20160922



VCCSA

220 0603 x13 (5 DV)



015/10/16 Modify (Power team request)

Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (Q4.5mD ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (Q4.5mD ESR)	Placed at backside side near to VR output
VCCGTx Power Plane at VR output	2x 220uF (Q4.5mD ESR)	Placed at primary side near to VR output
VCCDO Power Plane at VR output	1x 220uF (Q4.5mD ESR)	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

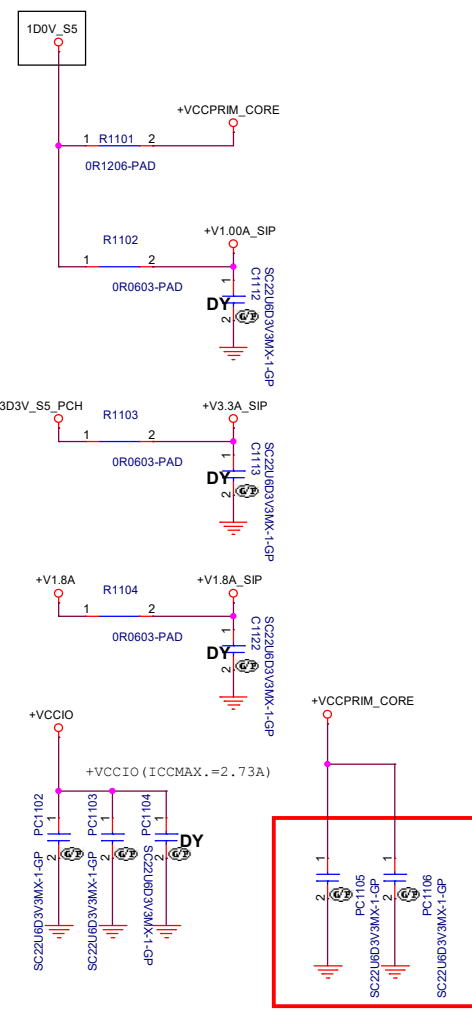
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 220uF 0402		Place on secondary side, underneath the package
VCCGT	7x 10uF 0402		Place as close to the package as possible
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
VDDQ	2x 10uF 0402		Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

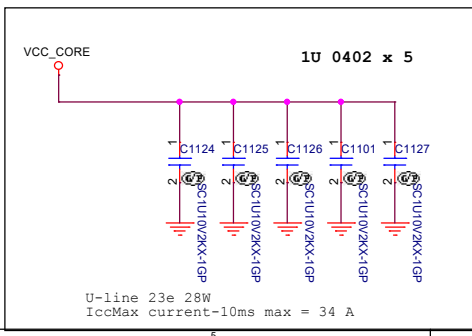
Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCSTP	2x 10uF 0402		Place on secondary side, underneath the package
VCCSTC	1x 10uF 0402		Place on secondary side, underneath the package

Main Func = CPU

PCH DERIVED RAILS

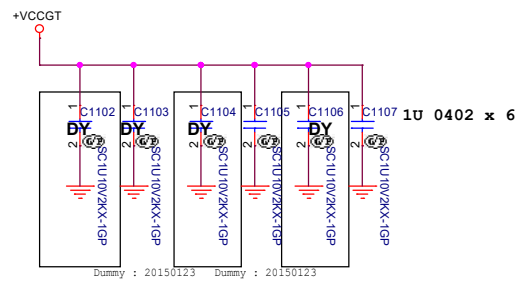


Size:0805 change to 0603
20141117

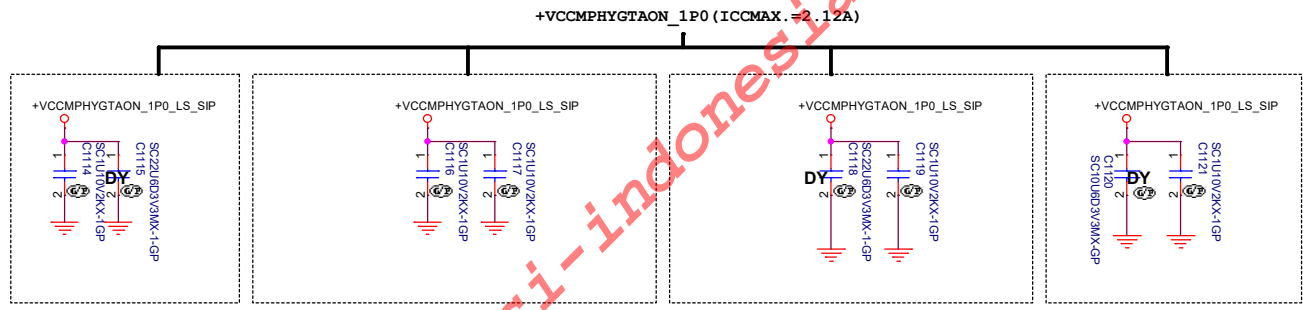
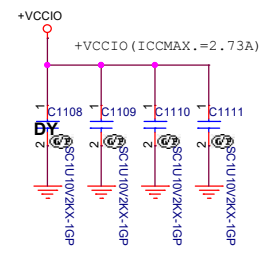


U-line 23e 28W
IccMax current-10ms max = 34 A

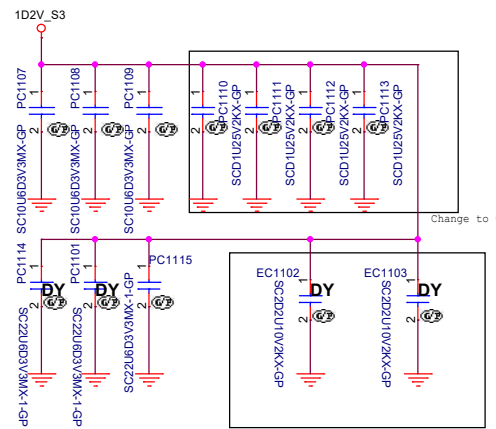
UNSLICED GT



VCCIO




Layout Note:
1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

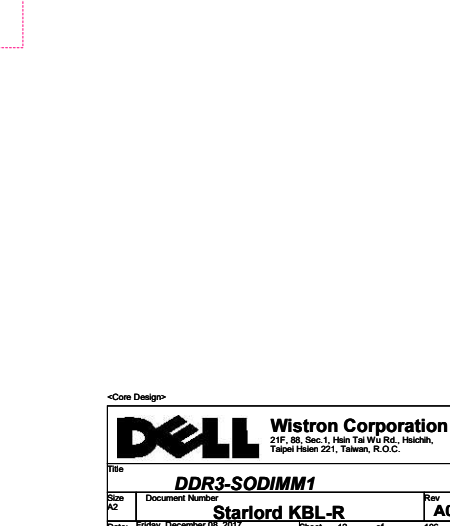
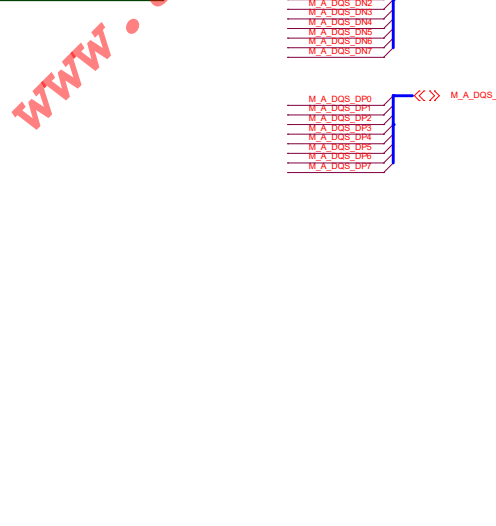
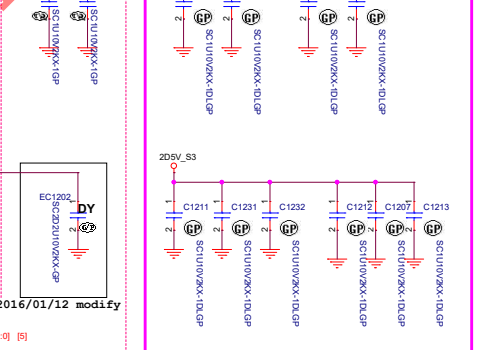
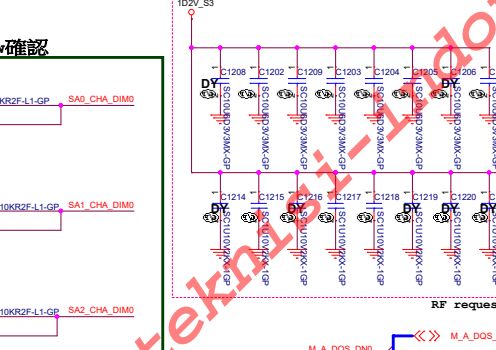
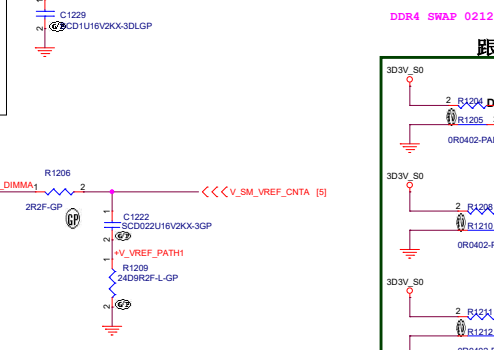
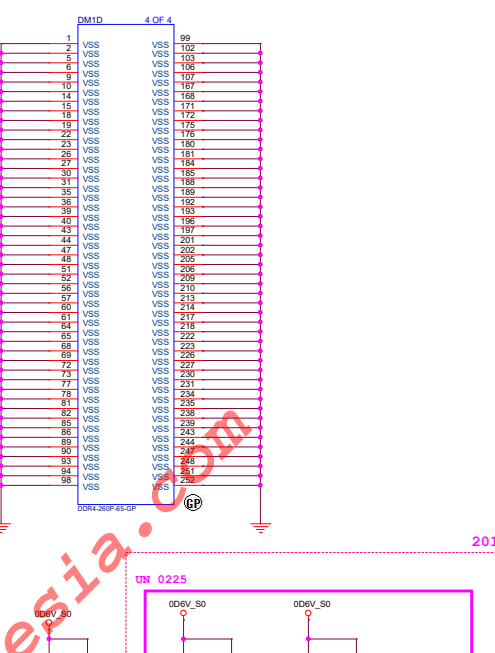
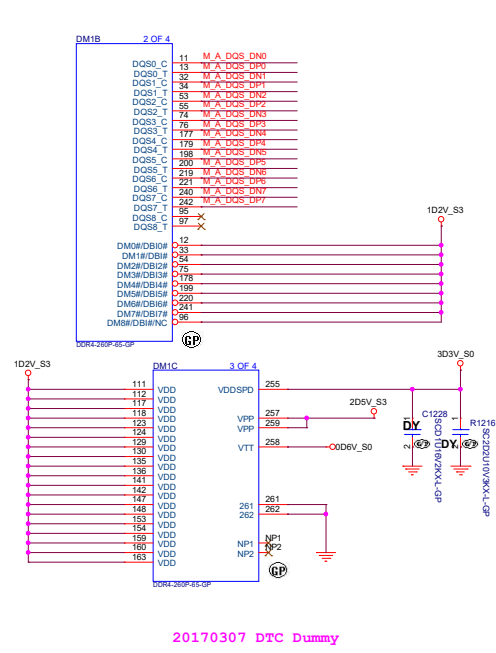
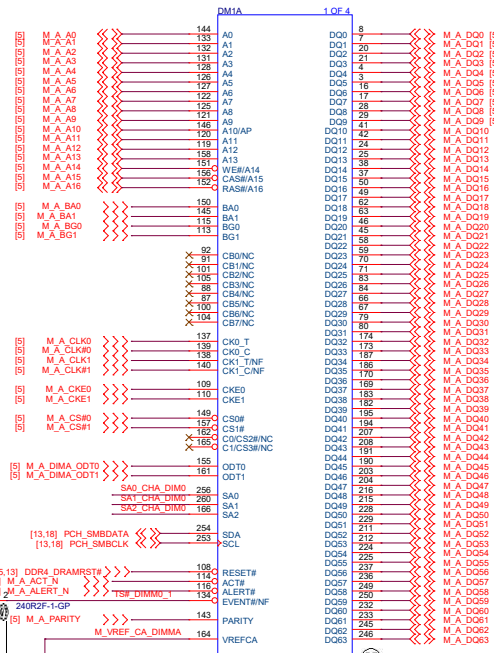


Change to 0.1uF at 20150427 for Power team

RF request 2016/01/12 modify

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Title CPU (Power CAP2)					
Size A3	Document Number Starlord KBL-R				Rev A00
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Title (Reserved)_SODIMM _SODIMM4		
Size A4	Document Number Starlord KBL-R	Rev A00
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The diagram shows a circuit for a 200R2F-Z-GP component. It includes a 150Ω resistor (R1502) connected to pin 2 of the component, which is then connected to ground. The component is labeled 200R2F-Z-GP.

GPIO Group Summary

GPIO Group	
Primary Well Group A (GPP_A)	
Primary Well Group B (GPP_B)	
Primary Well Group C (GPP_C)	
Primary Well Group D (GPP_D)	
Primary Well Group E (GPP_E)	
Primary Well Group F (GPP_F)	
Primary Well Group G (GPP_G)	
Deep Sleep Well Group (GPD)	

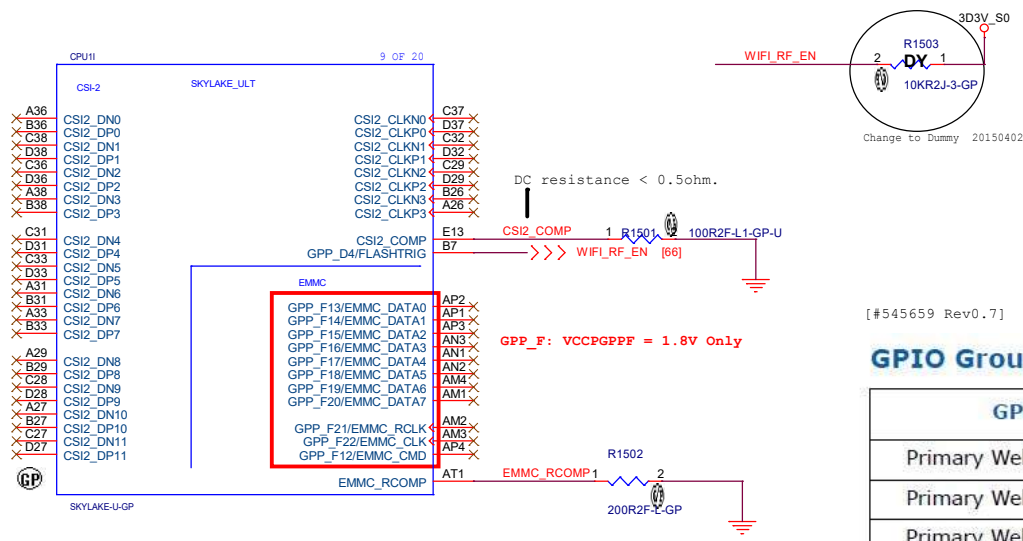


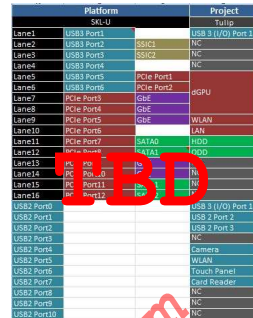
Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V



SKL	Max Device (Ports)	Max Lanes	PCIe Gen Type	Encoding	Transfer Rate (M/s)	Theoretical Max Bandwidth (GB/s)			
						x1	x2	x4	
U	6	12	1	8b/10b	2500	0.25	0.50	1.00	
			2	8b/10b	5000	0.50	1.00	2.00	
			3	128b/130b	8000	1.00	2.00	3.94	
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00	
			2	8b/10b	5000	0.50	1.00	2.00	

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x2	Port1				Port5				Port9			
	2x2	Port1	Port3			Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1	Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12	
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
	1x6	Port1				Port5							
W	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5	Port7	Port8					
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

[illegible]

	PCH-U HSIO Ports																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
	USB 3.1 (Optional or OTO)	USB 3.2 SSIC	USB 3.3	USB 3.4	USB 3.5 (Optional U- only)	USB 3.6 (Premium U- only) PCIe x2	PCIe x3	PCIe x4	PCIe x5	PCIe x6	PCIe x7 (Premium U- only) SATA 6G	PCIe x8 (Premium U- only) SATA 3.5	PCIe x9	PCIe x10	PCIe x11 SATA 4.8 (Optional)	PCIe x12 SATA 6.2 (Premium U- only)		
					X4		X4 [Intel RST for PCIe storage device #1]				X4 [Intel RST for PCIe storage device #2]							
					X2	X2		X2		X2		X2				X2		
CY17 Port Mapping	External Port /Type-C #1	External Port /Type-C #2 or WWAN SSIC	External Port /Type-C #3	External Port /Type-C #4 3D CAM	dGPU (x4)		LOM		WLAN		HDD (2.5")	ODD (2.5P) SSD (15P)	Thunderbolt Gen3x2 (Alpine Ridge SPALP)		Optane SSD/NVMe PCIe Gen3x4			
Starlord KBL Refresh	USB3.0 R1 (USB2)	USB3.0 R2_BDR (USB3)	N/A	Type-C #1 (USB1)	dGPU (x4)		WLAN		N/A	HDD1 (2.5")	N/A	M.2 SSD PCIe x4						

Main Func = PCH



Layout note: 3 PAD SHARING

EC1711 modify to 100k and 0.01uF at DVT1 20150203

SSID = PCH

PCH strap pin:

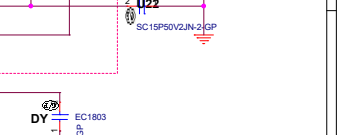
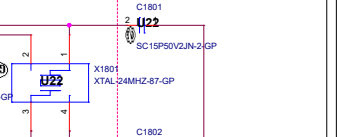
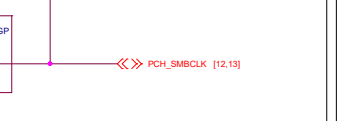
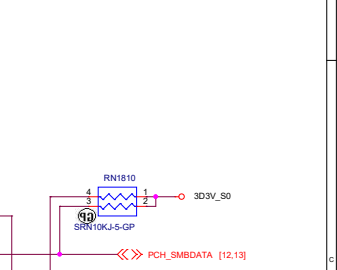
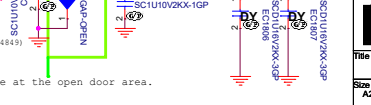
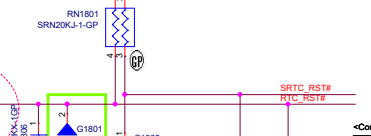
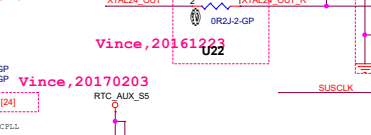
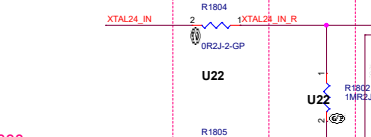
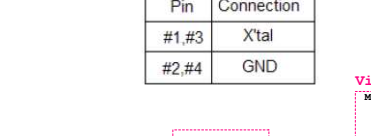
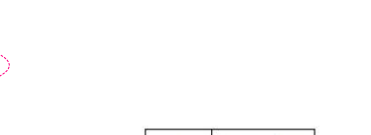
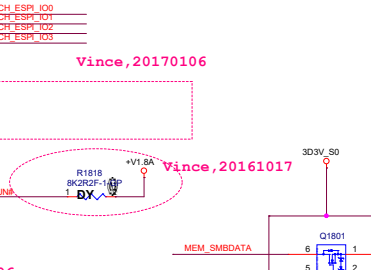
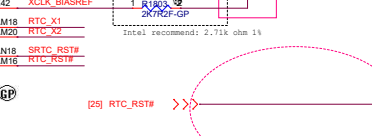
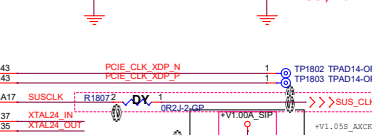
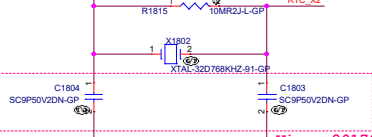
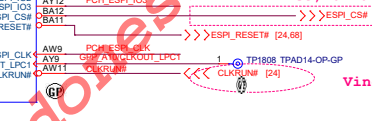
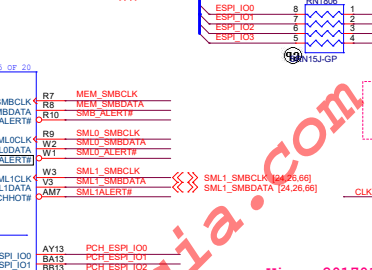
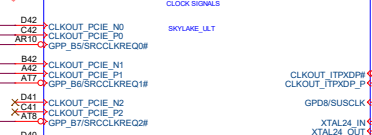
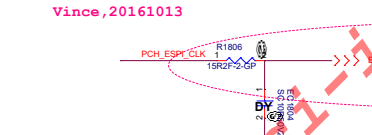
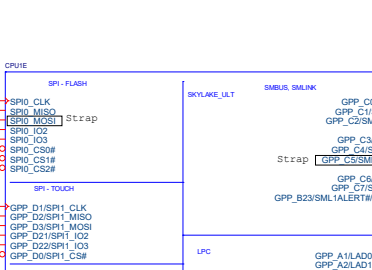
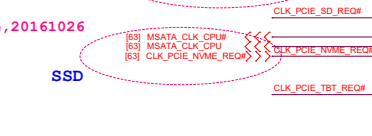
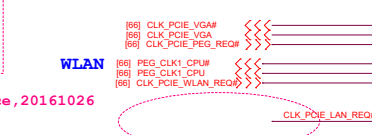
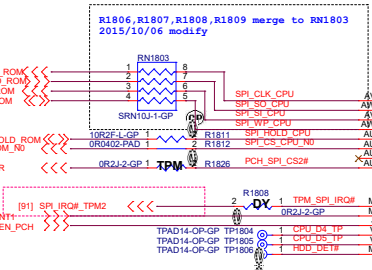
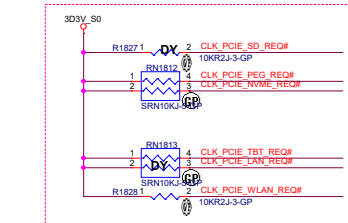
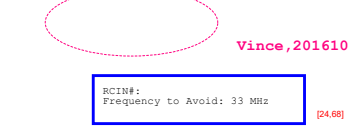
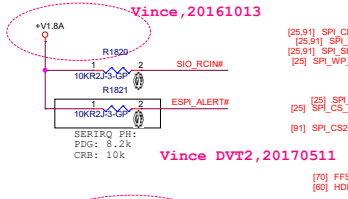
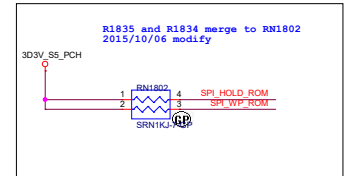
eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT#/ GPP_CS	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

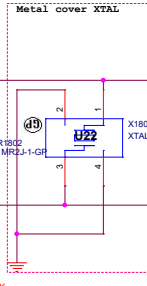
BOOT HALT	
SPIO_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

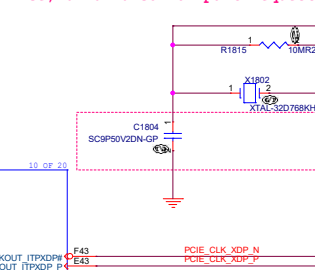


Pin	Connection
#1,#3	X'tal
#2,#4	GND

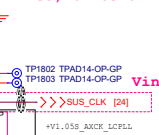
Vince,20170110



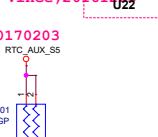
Vince,20170120 common part request



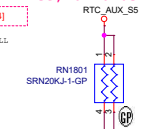
Vince,20170328



Vince,20161223



Vince,20170203



Vince,20161027



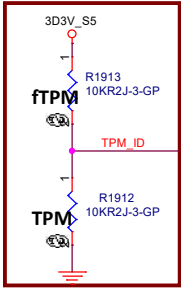
SSID = PCH

Strap pin:

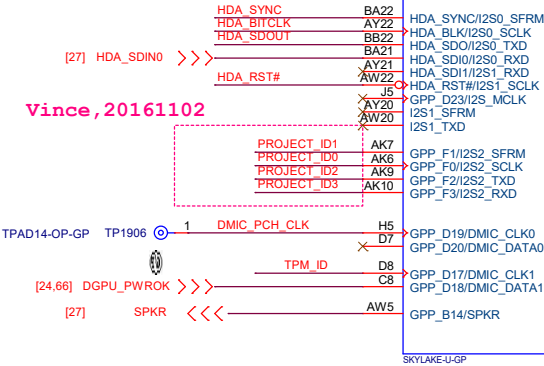
Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.

Vince,20161107



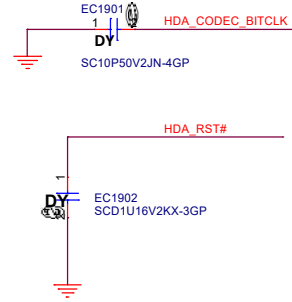
Vince,20161102



PCH strap pin:

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

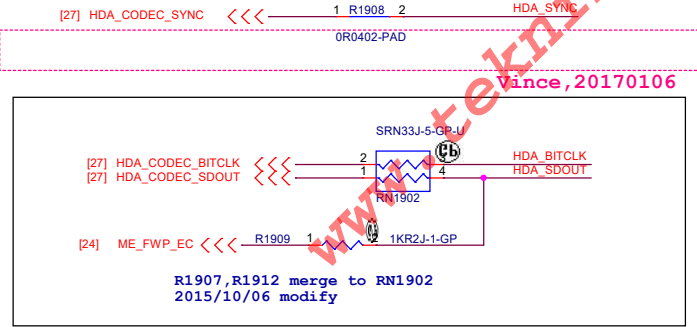
The internal pull-down is disabled after PLTRST# deasserts



PCH strap pin:

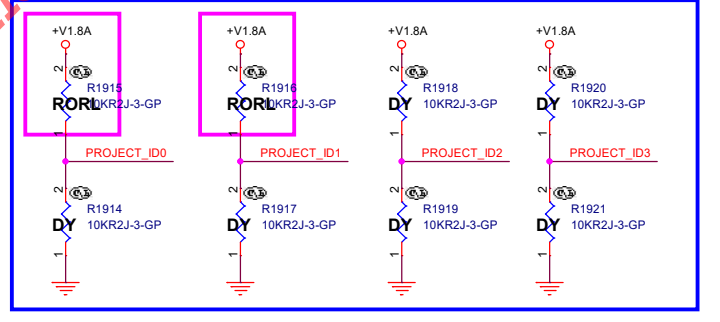
NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



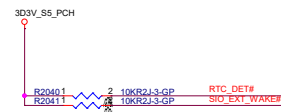
Vince,20170721

Vince,20170106



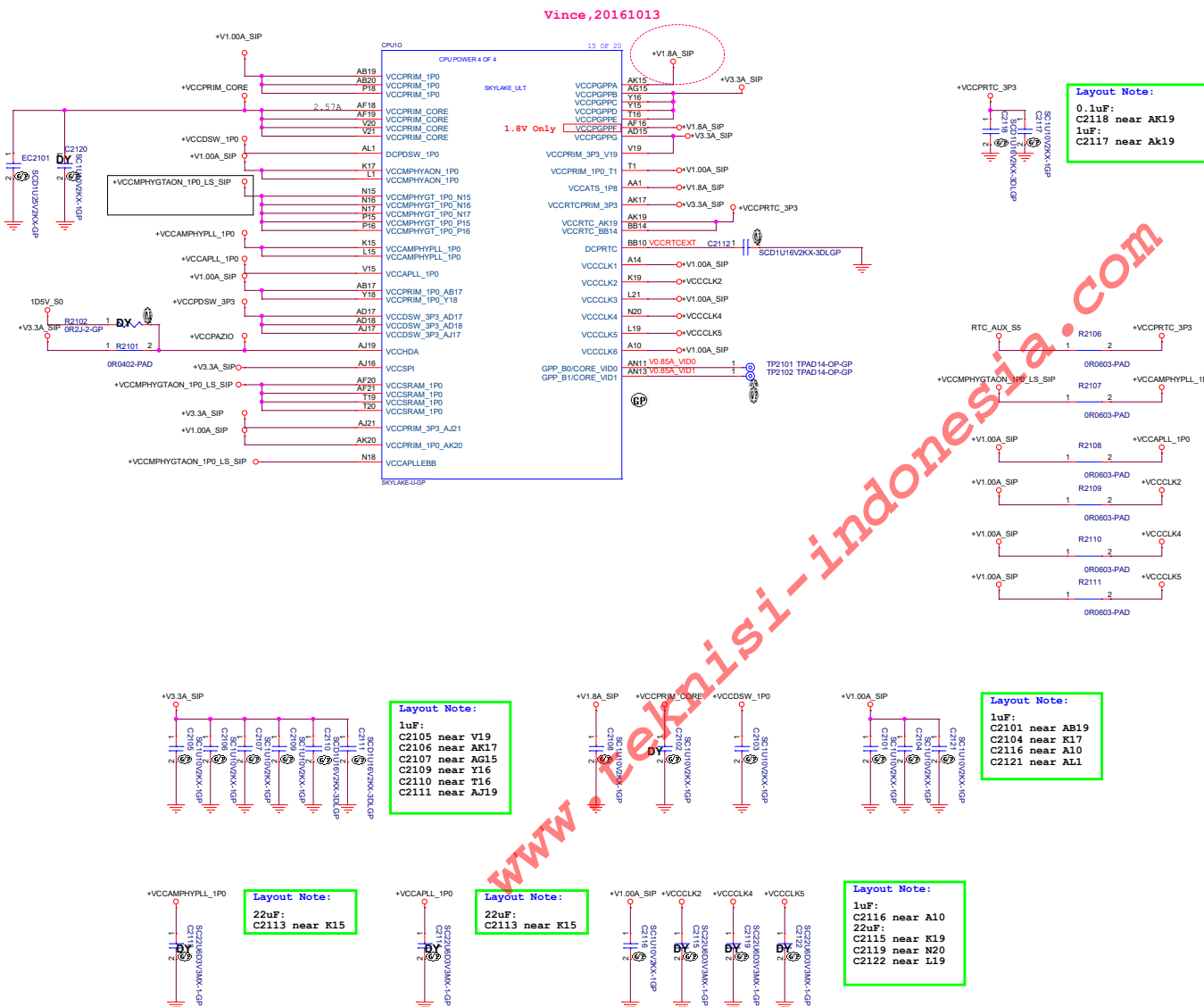
<Core Design>

SSID = PCH



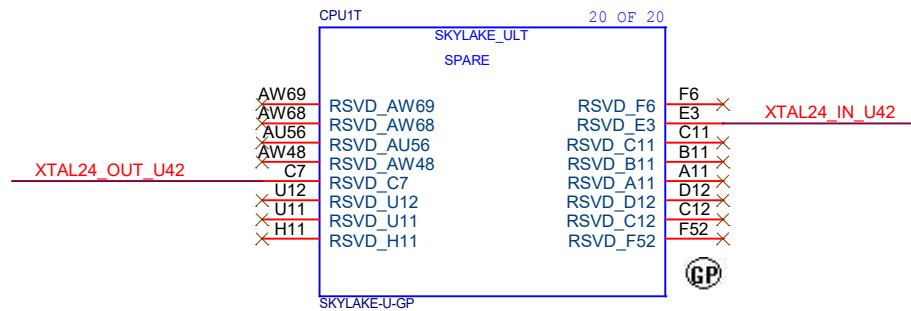
No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

BIOS strap pin:		GFP_C11
BIOS UMA/DIS Strap pin	BOARD_ID2	
UMA	0	
DIS	1	

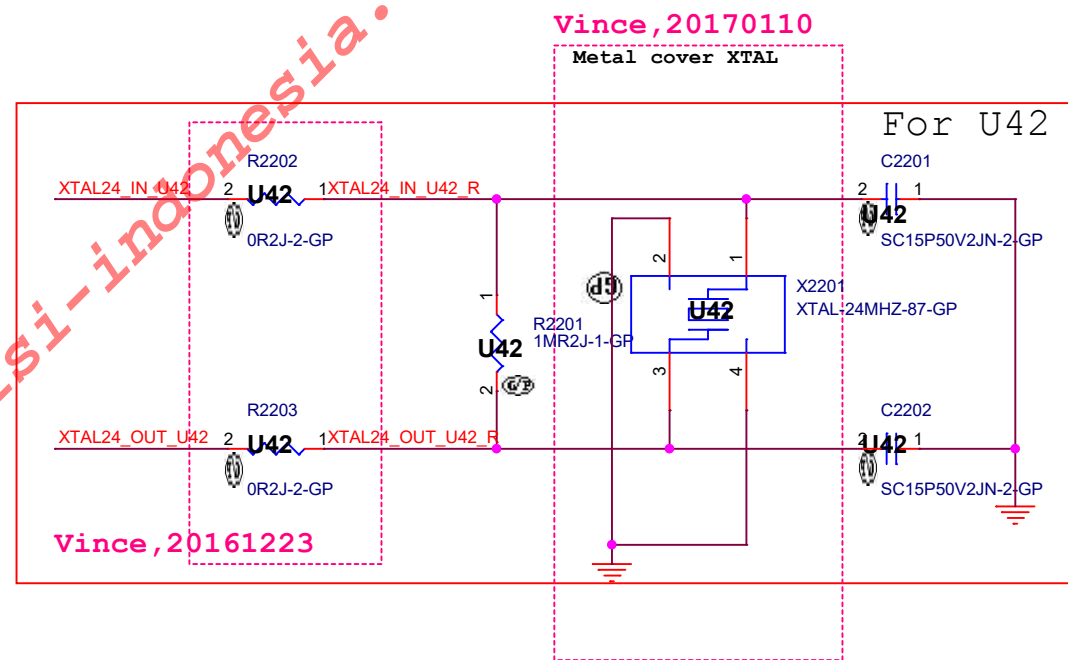


<Core Design>

Main Func = PCH



Pin	Connection
#1,#3	X'tal
#2,#4	GND



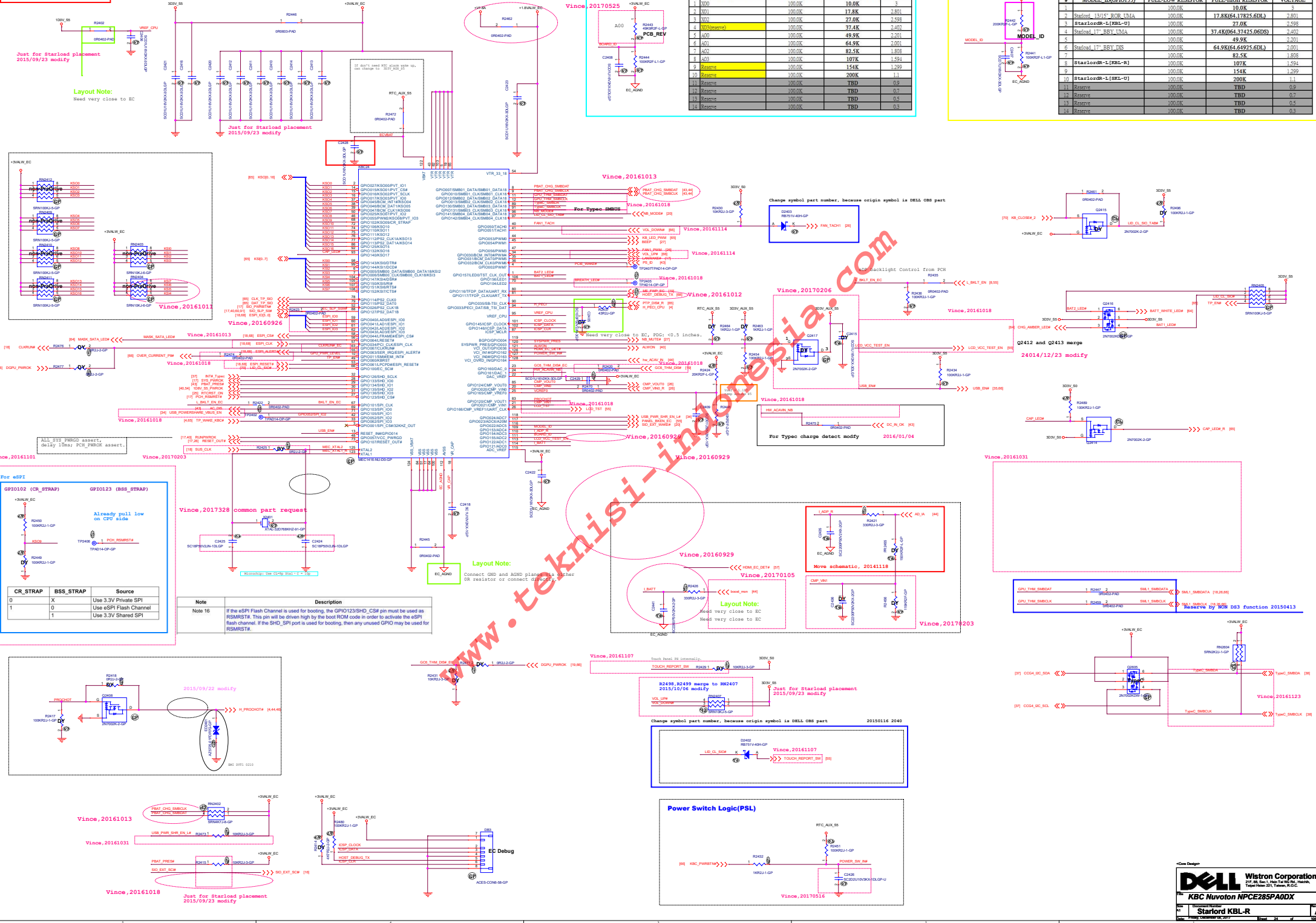
<Core Design>



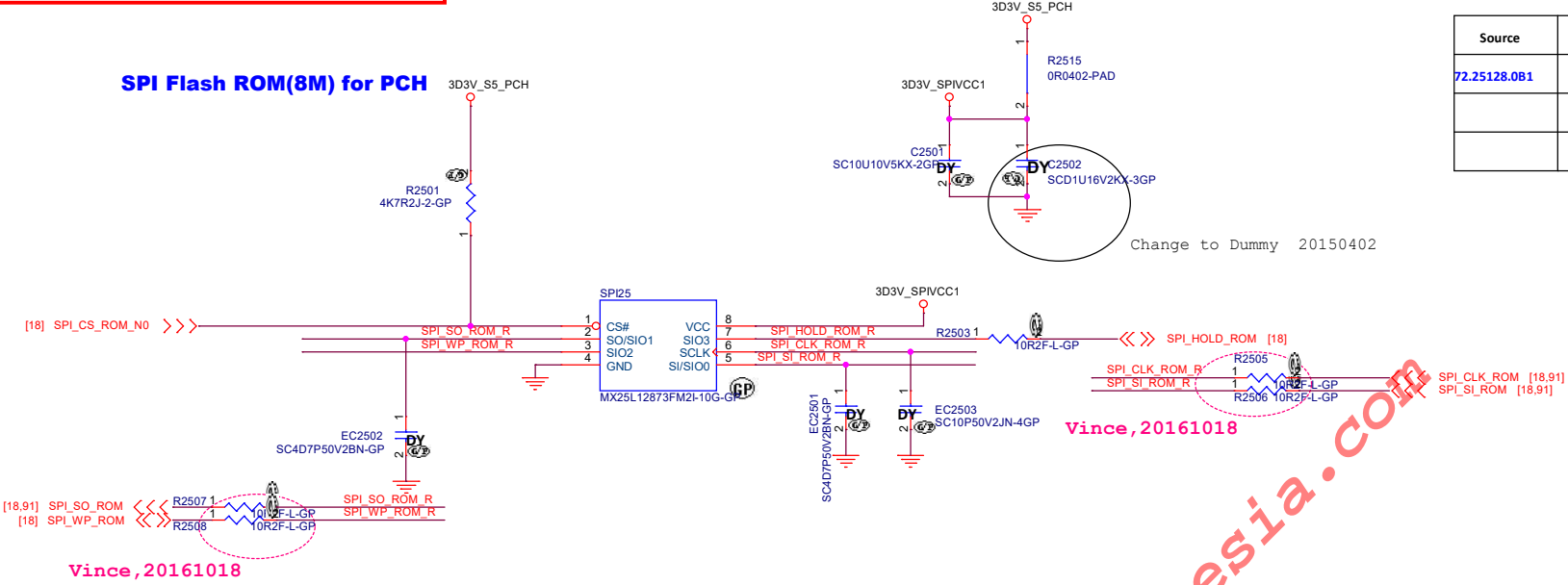
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU_(RSVD)		
Size A4	Document Number Starlord KBL-R	Rev A00
Date: Friday, December 08, 2017	Sheet 22 of 106	

Main Func = KBC



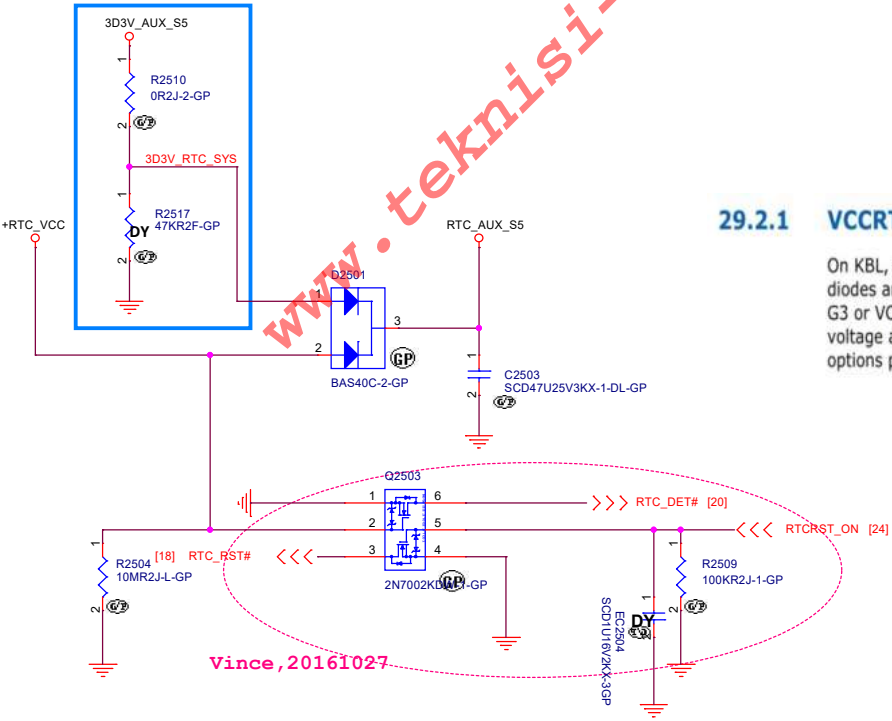
Main Func = SPI Flash



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25128.0B1	O	O	O
	O	O	O
	O	O	O

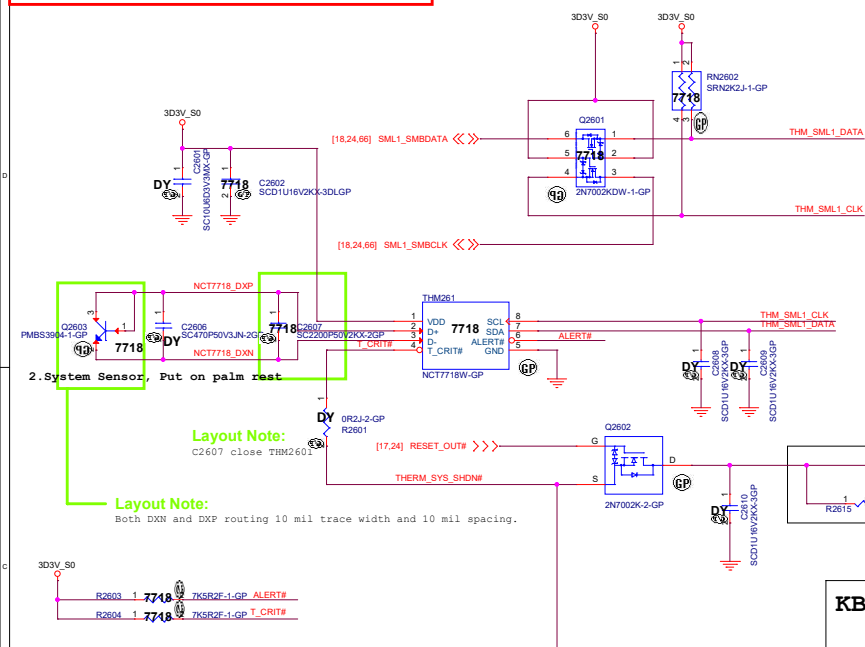
Delivery Voltage 3.19V
(when R2510 1K6 ohm)

Main Func = RTC



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



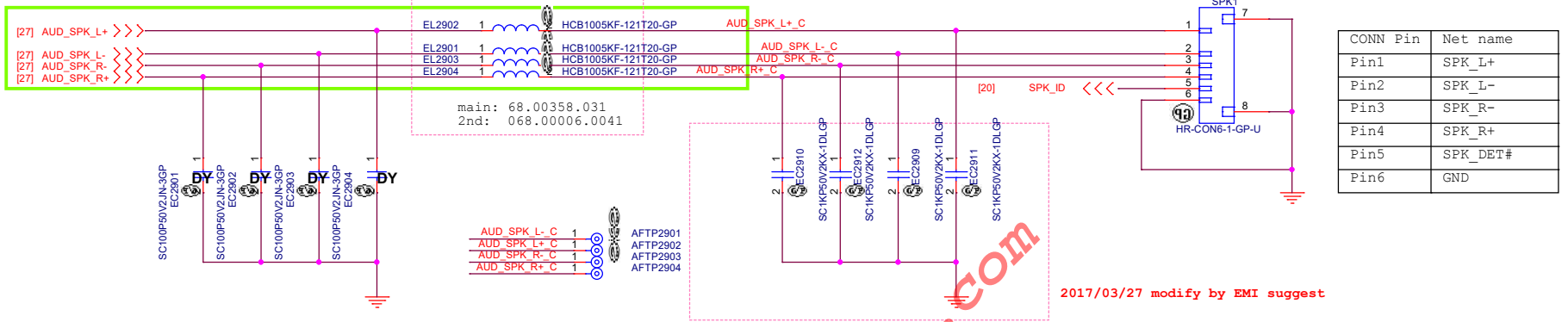
www.teknisi-indonesia.com

SSID = Audio

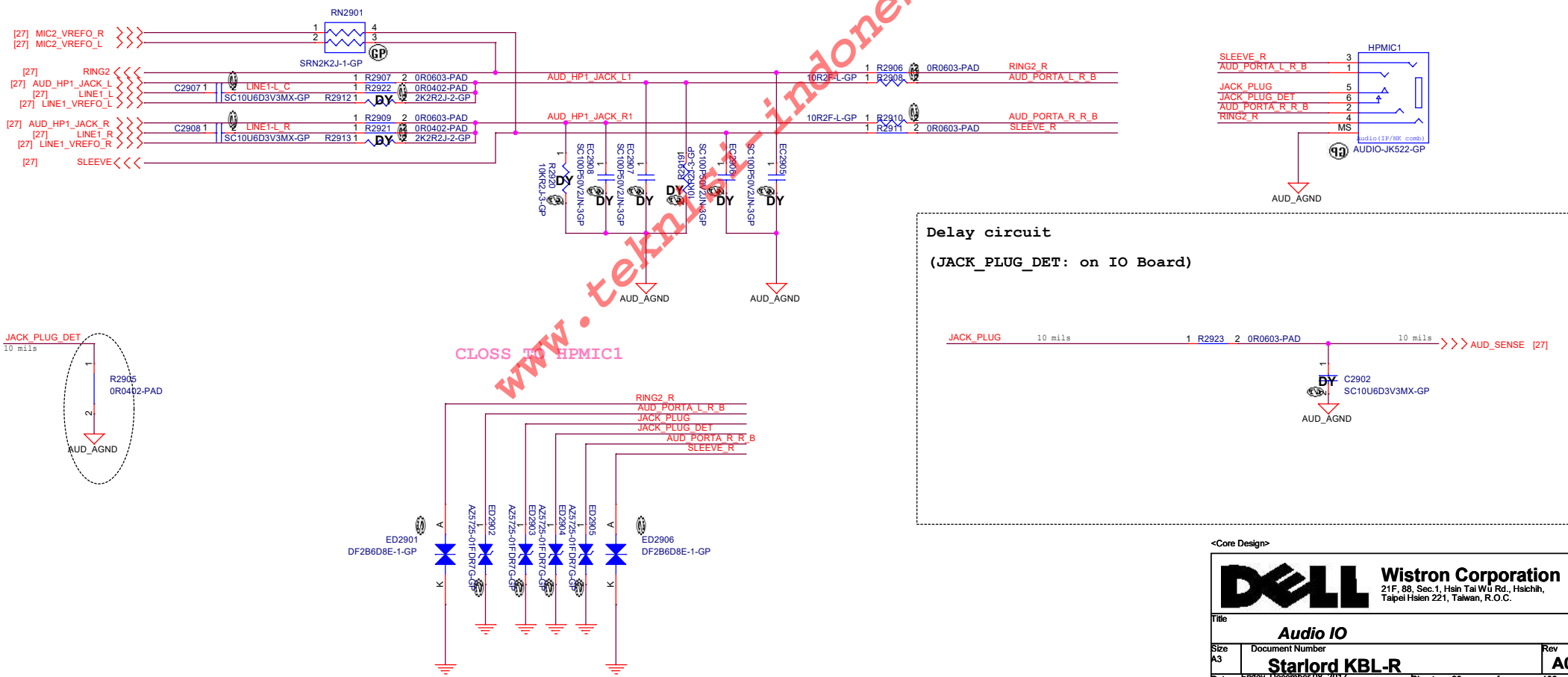
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



Universal Jack (Moved to I/O Board)



Main Func = Audio

(Blanking)

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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Starlord KBL-R		Rev A00
Date: Monday, August 28, 2017		Sheet 30 of	106

(Blanking)


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SSID = LAN

(Blanking)

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<Core Design>



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Title

XFOM&RJ45

Size	Document Number	Rev
A3	Starlord KBL-R	A00

Date: Monday, August 28, 2017	Sheet 32 of 106
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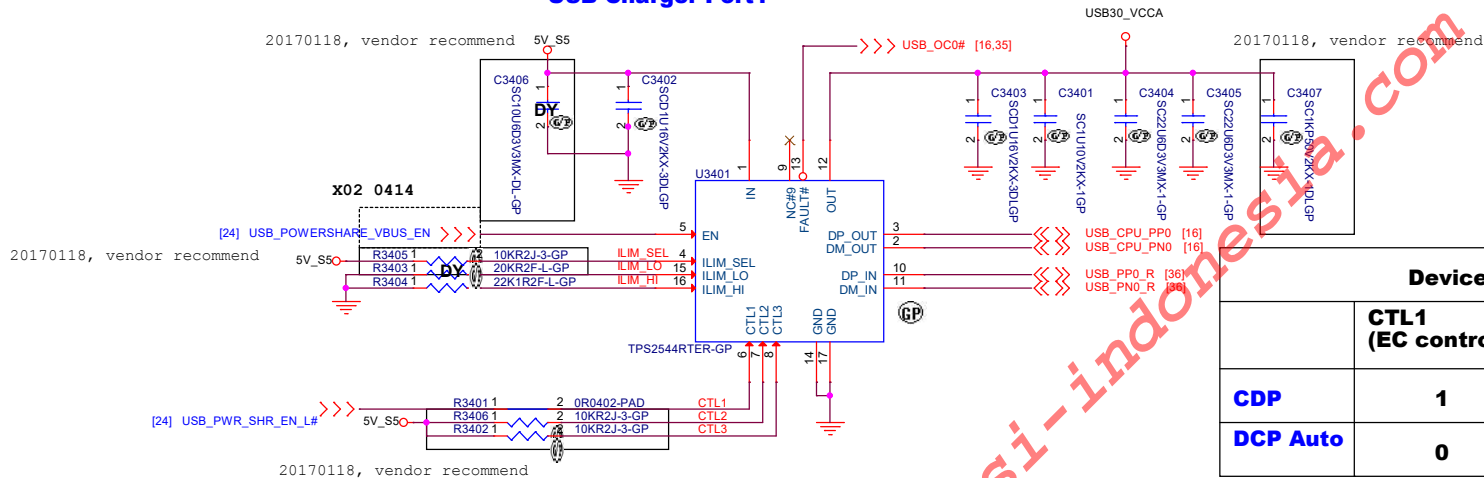
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<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Card Reader-RTS5170					
Size	Document Number				Rev
A2	Starlord KBL-R				A00
Date: Monday, August 28, 2017					
Sheet 32 of 108					

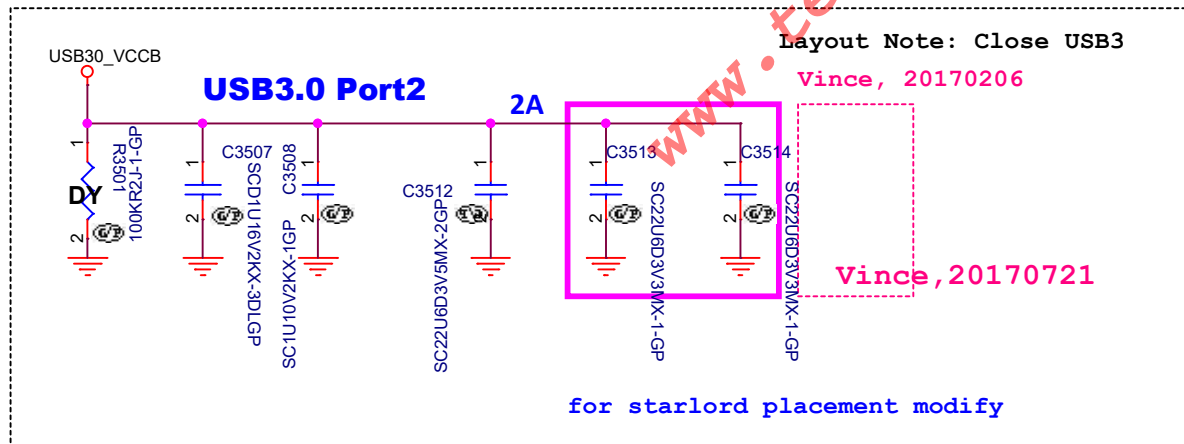
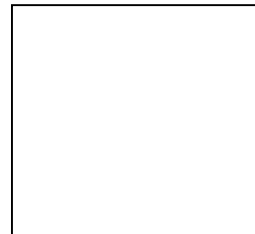
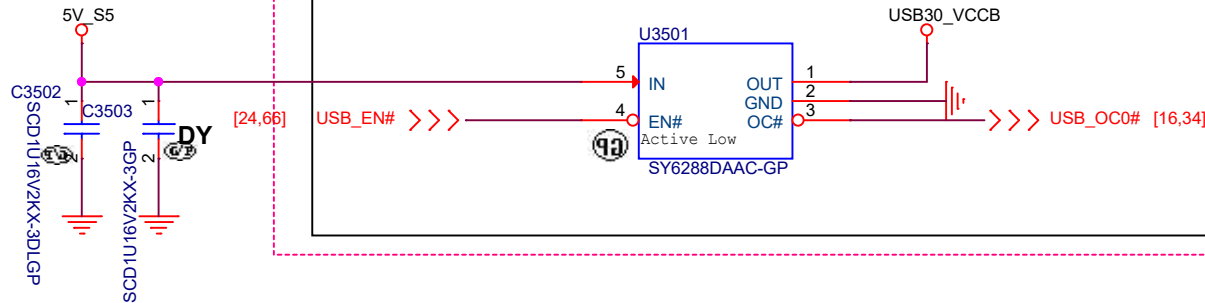
USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

Main Func = USB3.0 Port1

Vince, 20170206



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB switch

Size

Document Number

Starlord KBL-R

Rev

A00

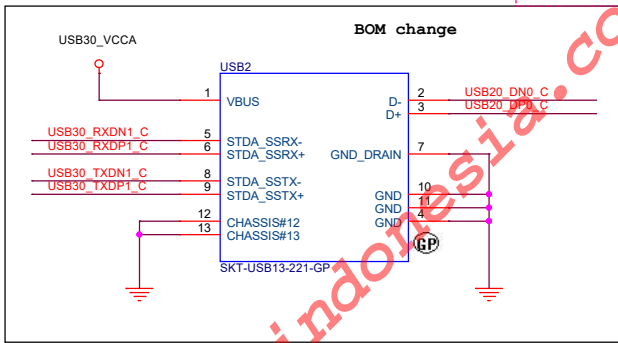
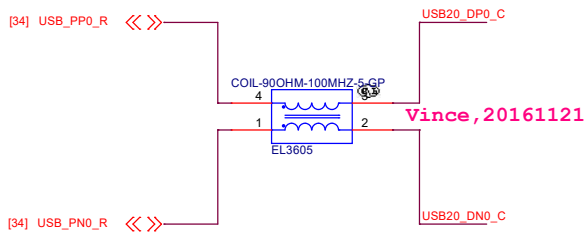
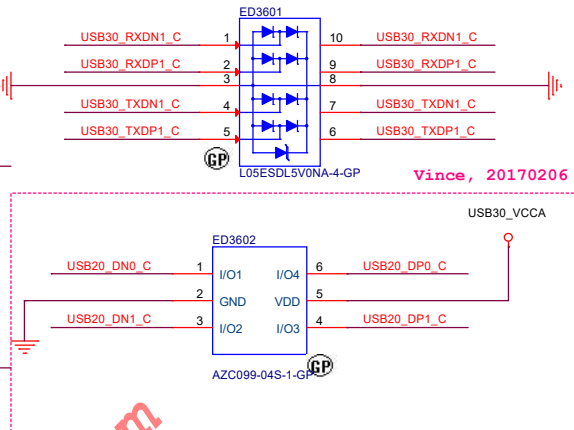
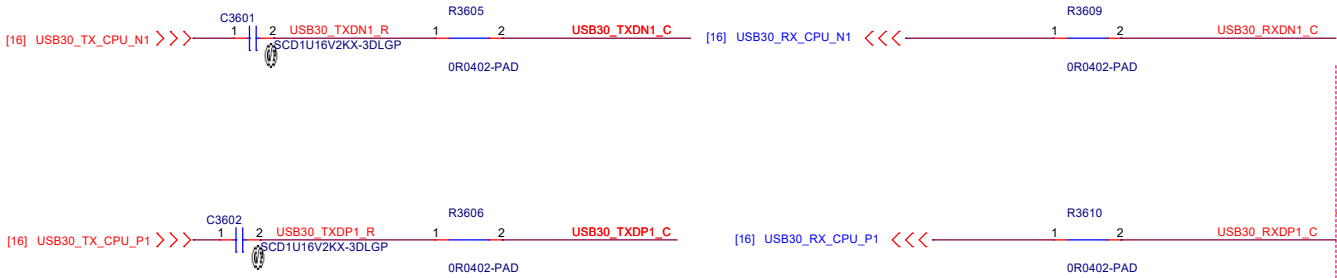
Date: Friday, December 08, 2017

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SSD = USB3.0 Port1

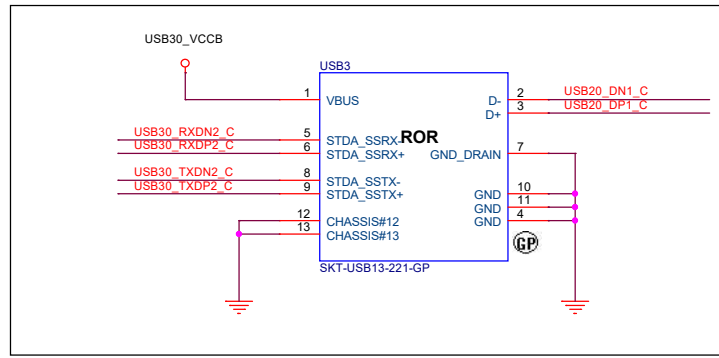
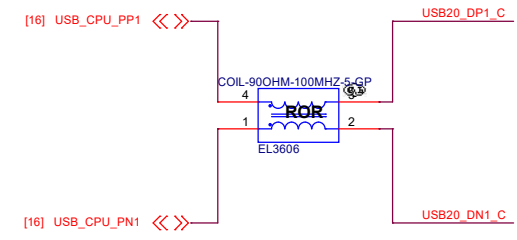
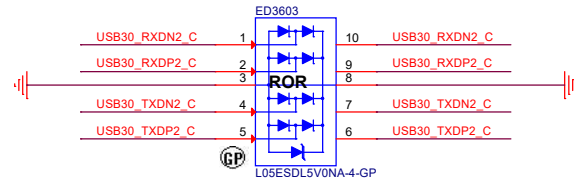
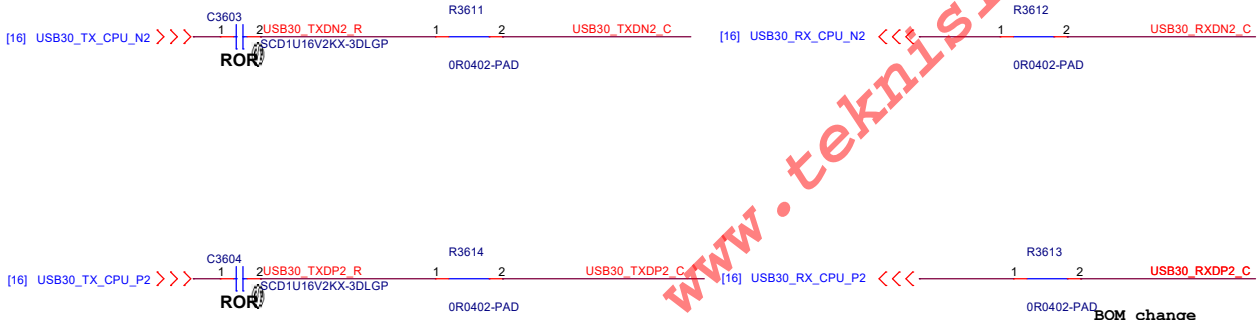
USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Port2



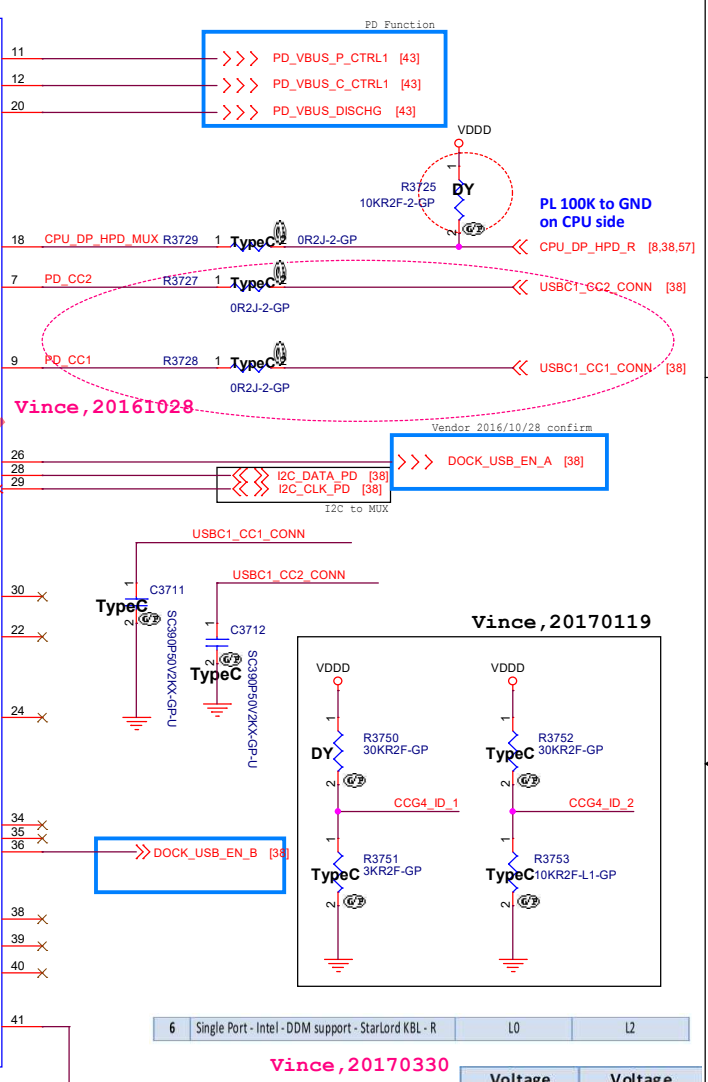
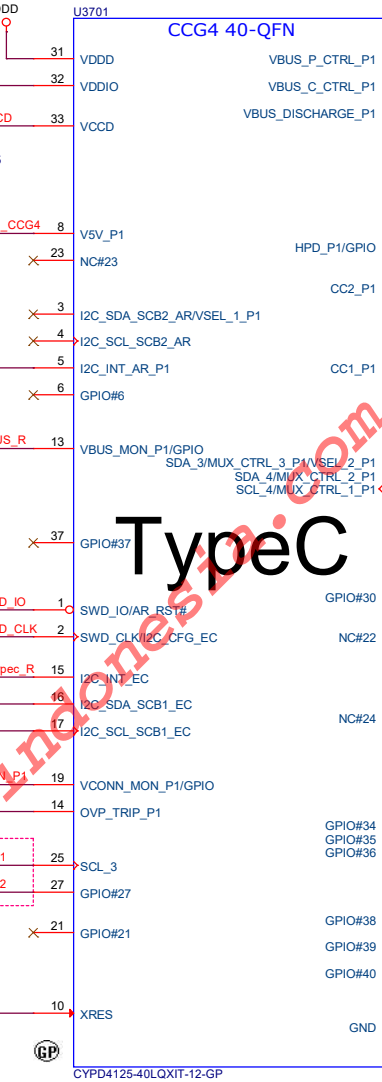
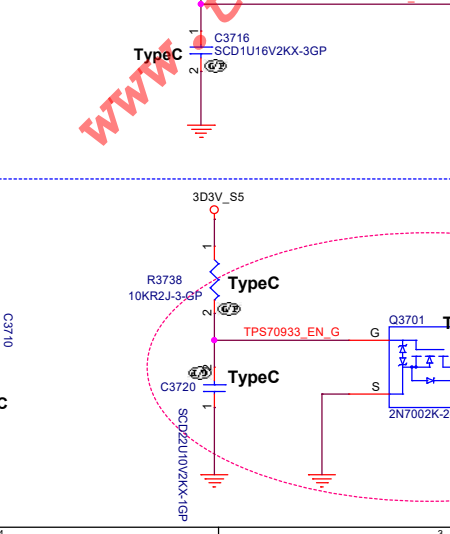
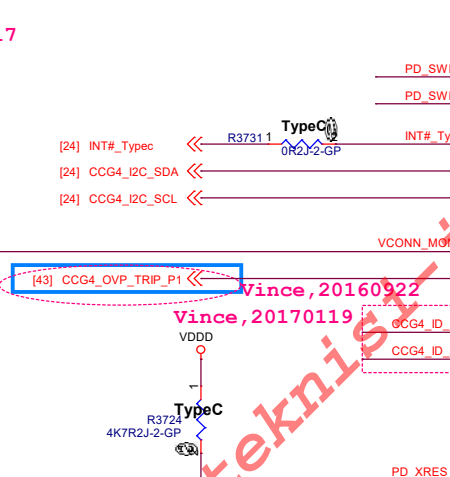
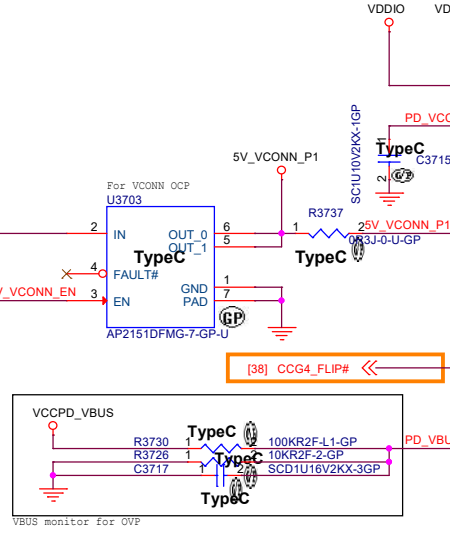
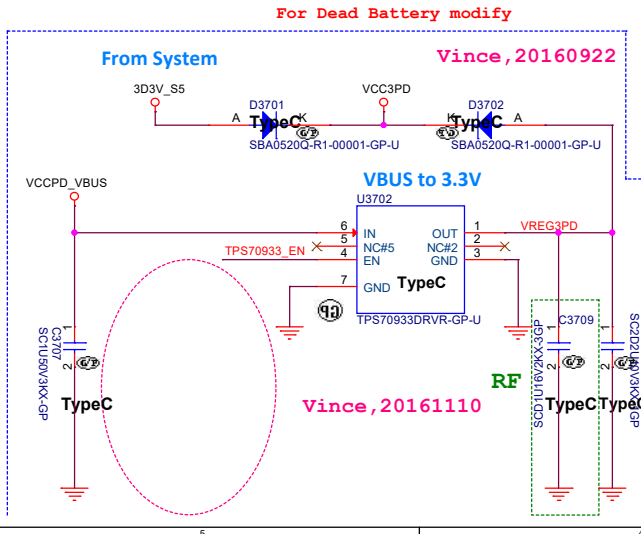
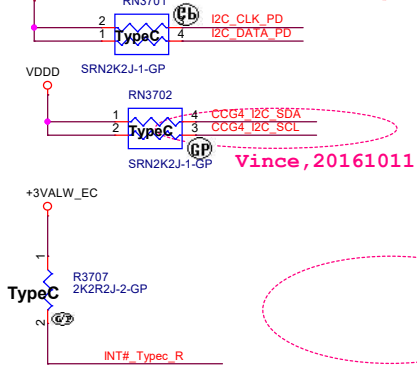
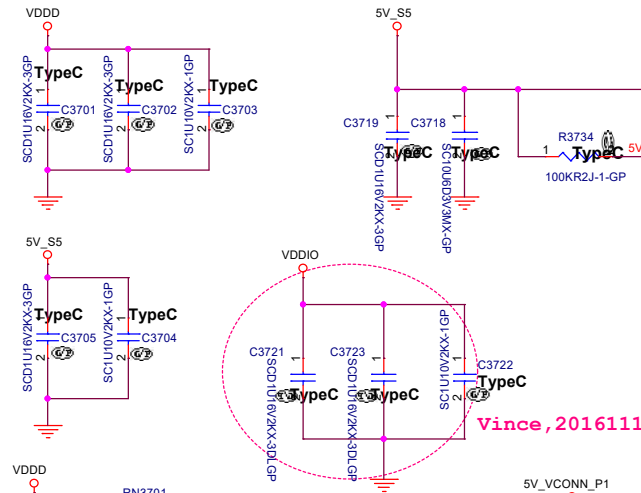
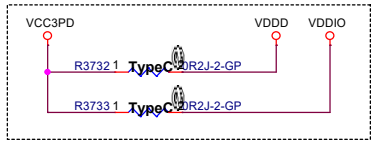
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Title: **USB30**

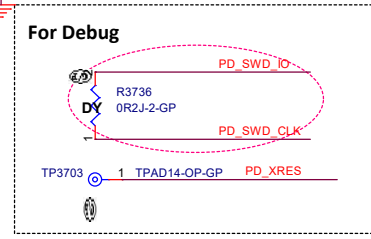
Size A3 Document Number: **Starlord KBL-R** Rev: **A00**

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TypeC

6	Single Port - Intel - DDM support - Starlord KBL - R	L0	L2
---	--	----	----



Voltage level	Voltage value
L0	0V
L1	3.3V/8
L2	2 * 3.3V/8
L3	3 * 3.3V/8
L4	4 * 3.3V/8
L5	5 * 3.3V/8
L6	6 * 3.3V/8
L7	7 * 3.3V/8

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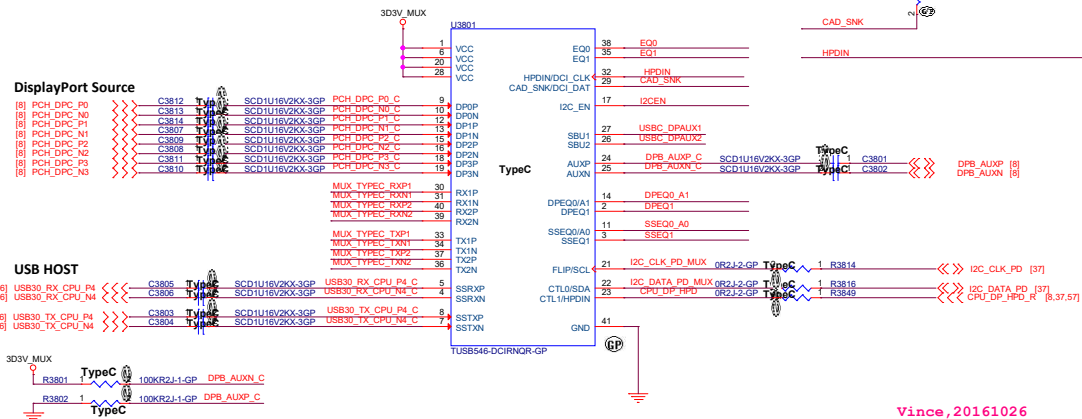
Starlord KBL-R

Rev A00

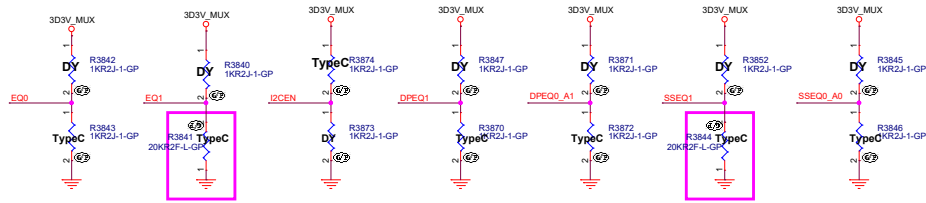
Date: Friday, December 08, 2017 Sheet 37 of 106

Main Func = TYPEC MUX

Vince, 20161012



Vince, 20161026



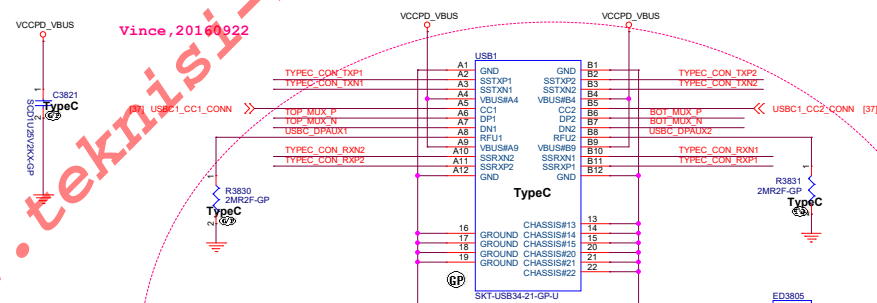
Vince, 20170721

Vince, 20170721

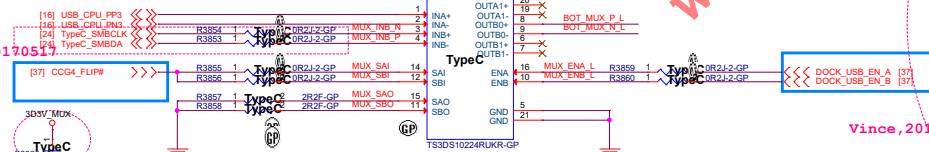
FLIP POL	CE10 AMSEL	CE11 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI	non-DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable in GPIO mode, Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI CLK in I2C mode	HPD

Vince, 20160922

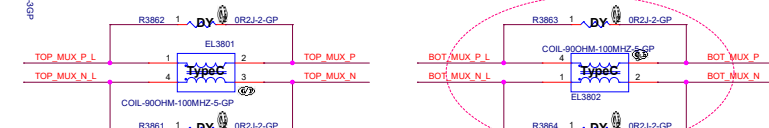


Vince, 20161028

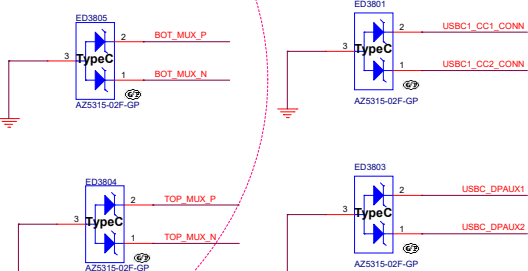
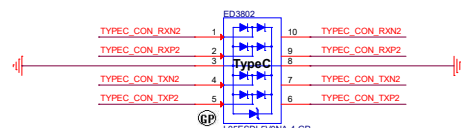
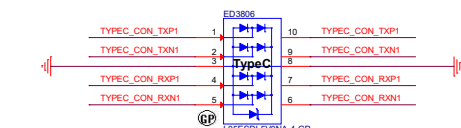


Vince, 20161004

Vince, 20160929



FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C



<Core Design>

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Title			
(Reserved)			
Size A2	Document Number Starlord KBL-R		Rev A00
Date: Friday, December 08, 2017		Sheet 38 of 106	

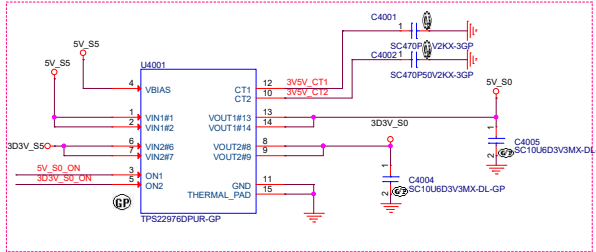
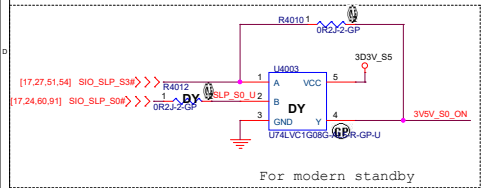
Main Func = USB3.0 Port1

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SSID = Power Plane & Sequence

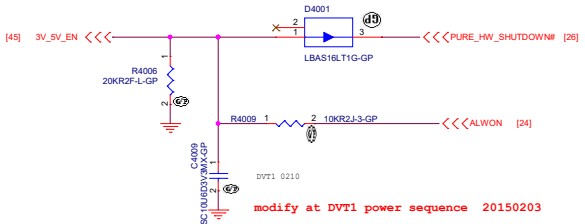
ROSA Run Power

change common part PN:074.05027.0093, 20170110



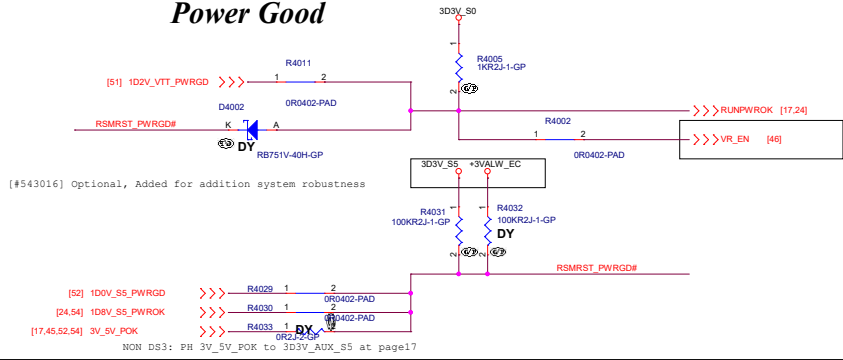
5V_S0

5V_S0 Consumption
Peak current 5A
3D3V_S0
3D3V_S0 Consumption
Peak current 2.5A

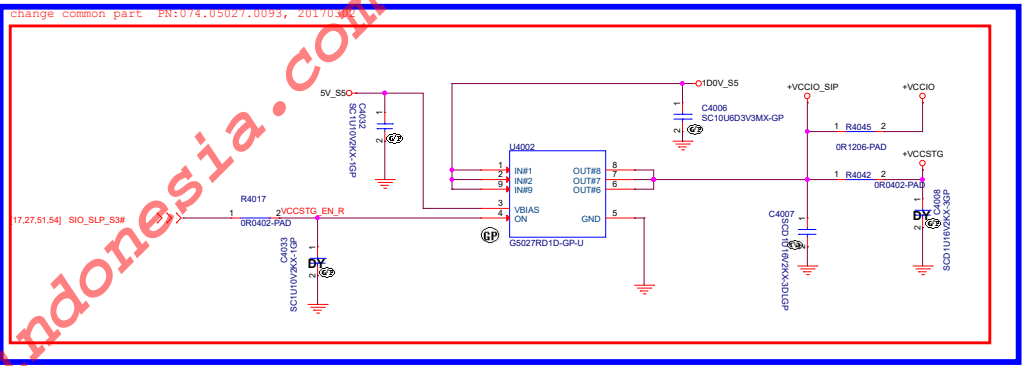


20150116 2032

Power Good



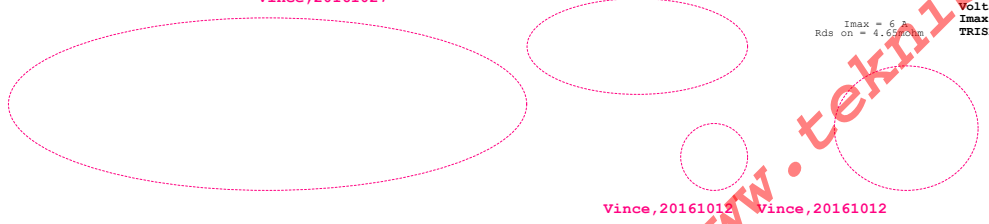
VCCIO and VCCSTG



EOPIO and EDRAM

Vince,20161012

Vince,20161012



+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

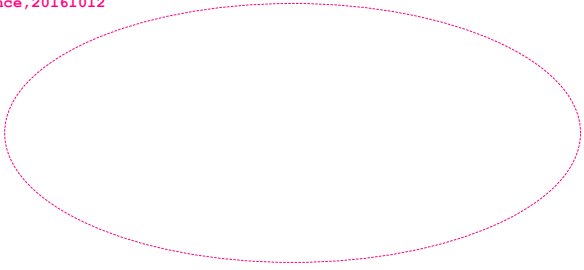
+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

Vince,20161012

V1.8S

Vince,20161012

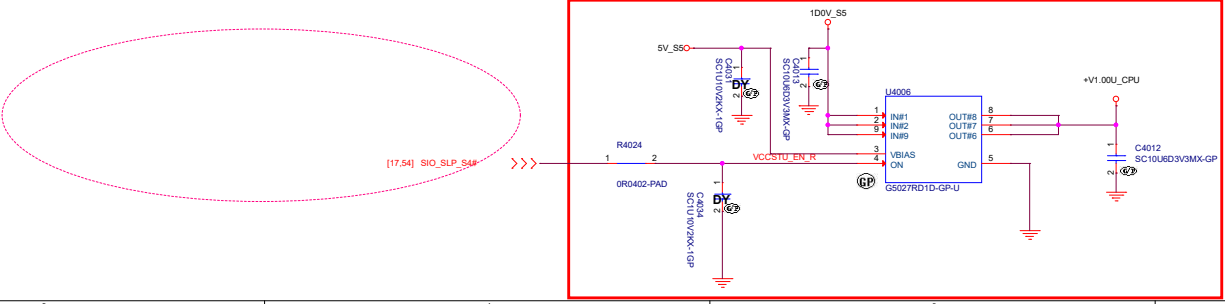


MANAGEMENT RAIL POWER GENERATION

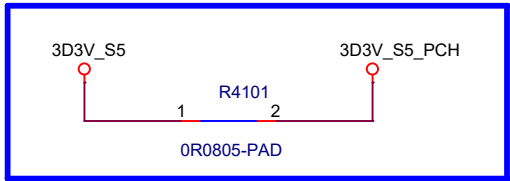
VCCSTG, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST

change common part PN:074.05027.0093, 20170110



Main Func = Power Plane & Sequence




Reserve by NON DS3 function 20150413

Vince,20161031

DS3

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Title Connected_Standby(1/2)+DS3			
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Main Func = DIMM1
Main Func = DIMM2

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Title

Connected_Standby(2/2)

Size

Document Number

Rev

A3

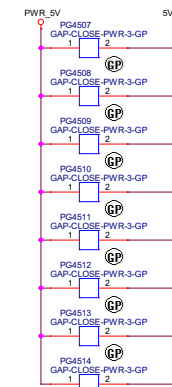
Starlord KBL-R

A00

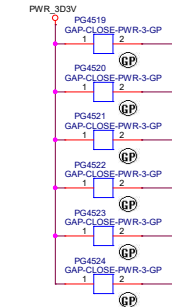
Date: Monday, August 28, 2017

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SSID = PWR.Plane.Regulator_3D3V
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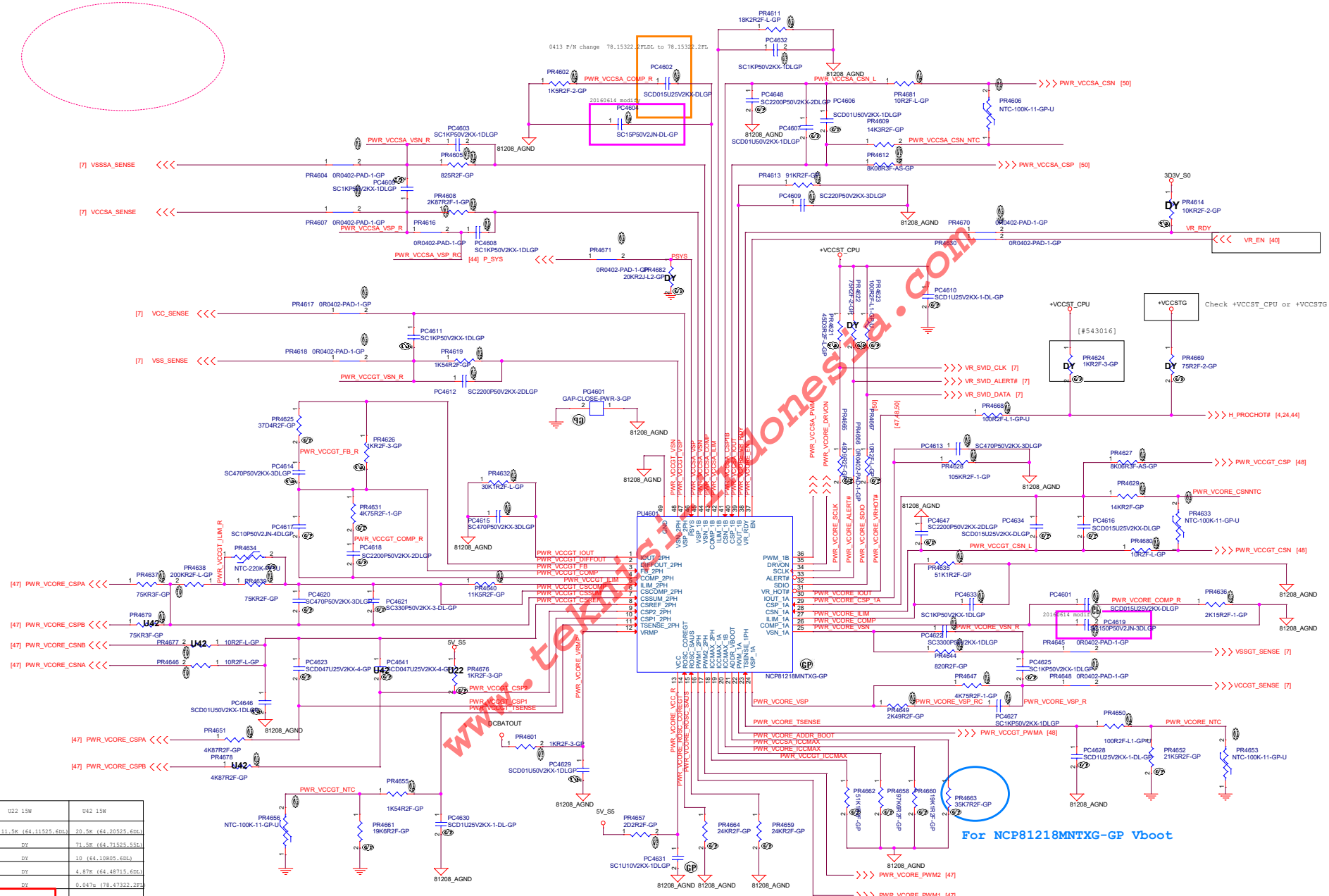
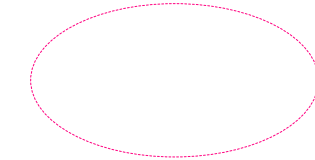


Design Current=5A
7.5A<OCP>9A



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	U22 15W	U42 15W
PR4640	51.5K (64.11525,60L)	20.3K (64.20525,60L)
PR4678	DY	71.5K (64.71525,55L)
PR4677	DY	10 (64.10005,60L)
	DY	4.87K (64.48715,50L)
PC4641	DY	0.047K (64.04722,22F)
PR4676	1K (64.10055,60L)	17K (64.17022,22F)
PR4662	51.1K (64.51125,60L)	100K (64.10035,60L)
PR4658	97.6K (64.97625,60L)	97.6K (64.97625,60L)
PR4635	51.1K (64.51125,60L)	51.1K (64.51125,60L)
PR4628	105K (64.10535,60LLS)	105K (64.10535,60LLS)
PR4632	30.3K (64.30325,60L)	28.3K (64.28325,60L)

20170208

For NCP81218MNTXG-GP Vboot

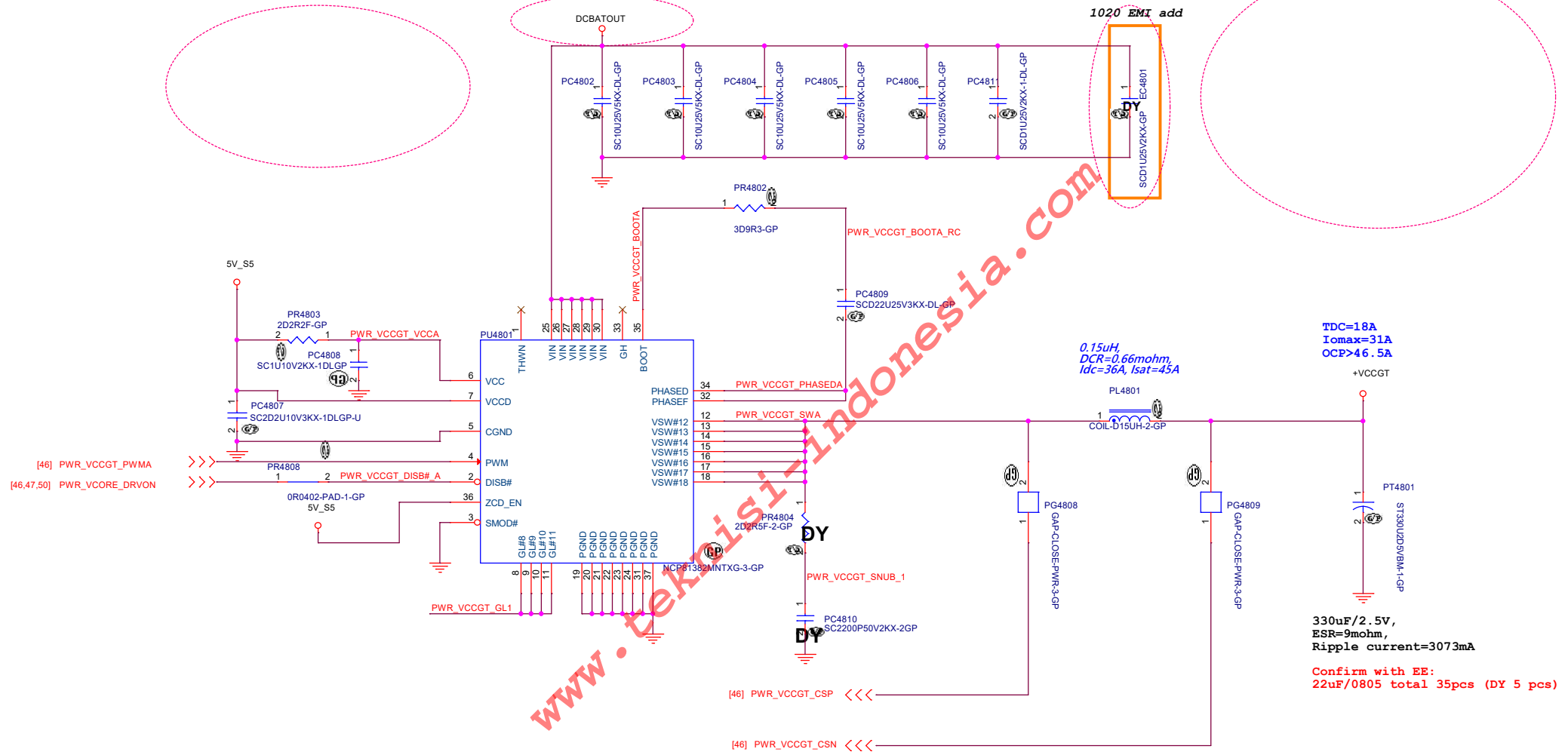
Main Func = CPU CORE

Vince, 20160922

Vince, 20160929

Vince, 20161020

Vince, 20160929



<Core Design>




Main Func = CPU_CORE

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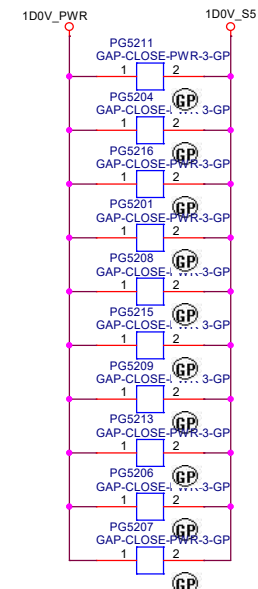
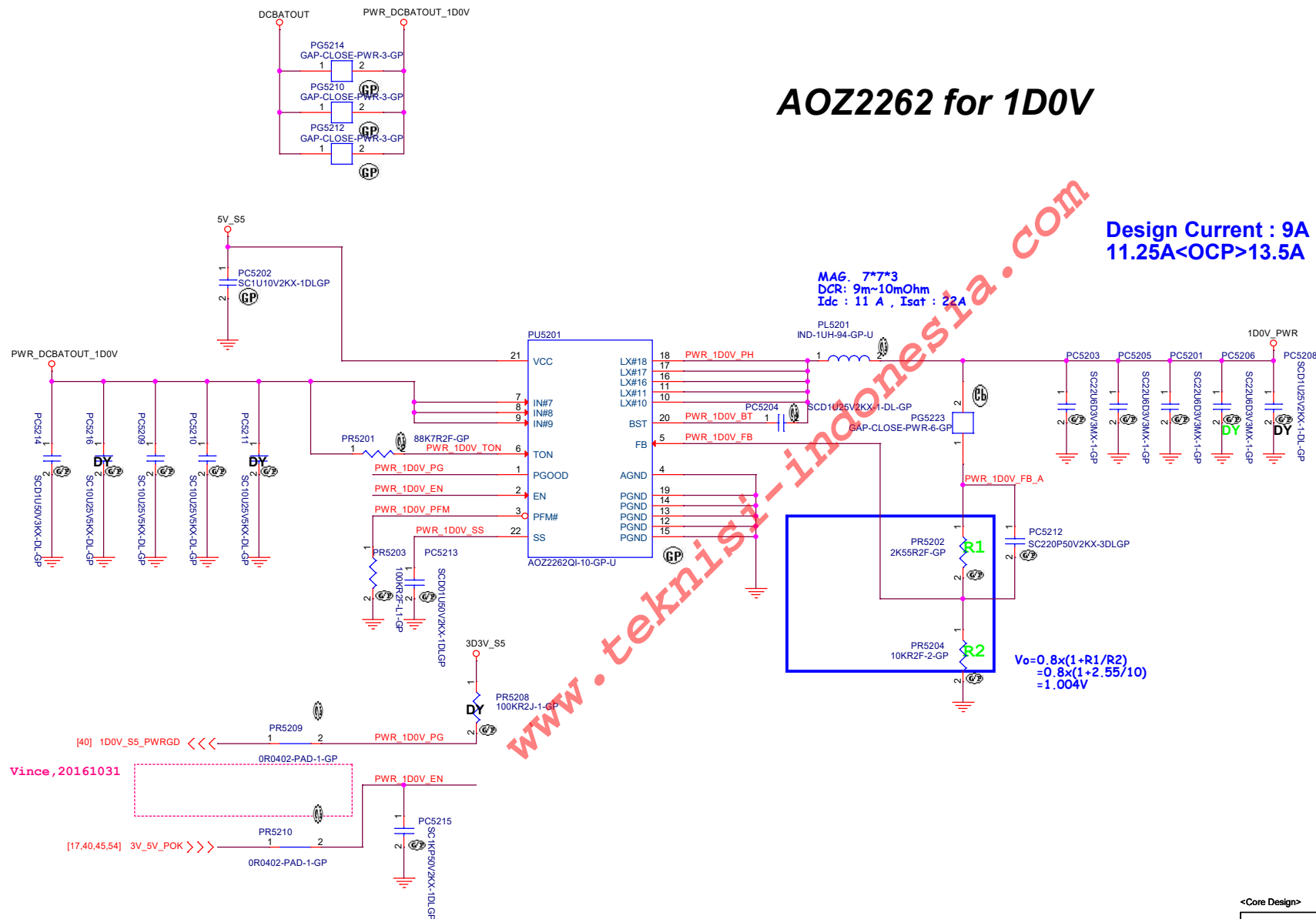
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Title NCP81210MN_CPU_VCCGTUS			
Size A4	Document Number Starlord KBL-R		Rev A00
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```
SSID = PWR.Plane.Regulator_1D0V
```

AOZ2262 for 1D0V

Design Current : 9A
11.25A<OCP>13.5A



<Core Design>



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(Reserved)

Size
A3

Document Number	
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Title

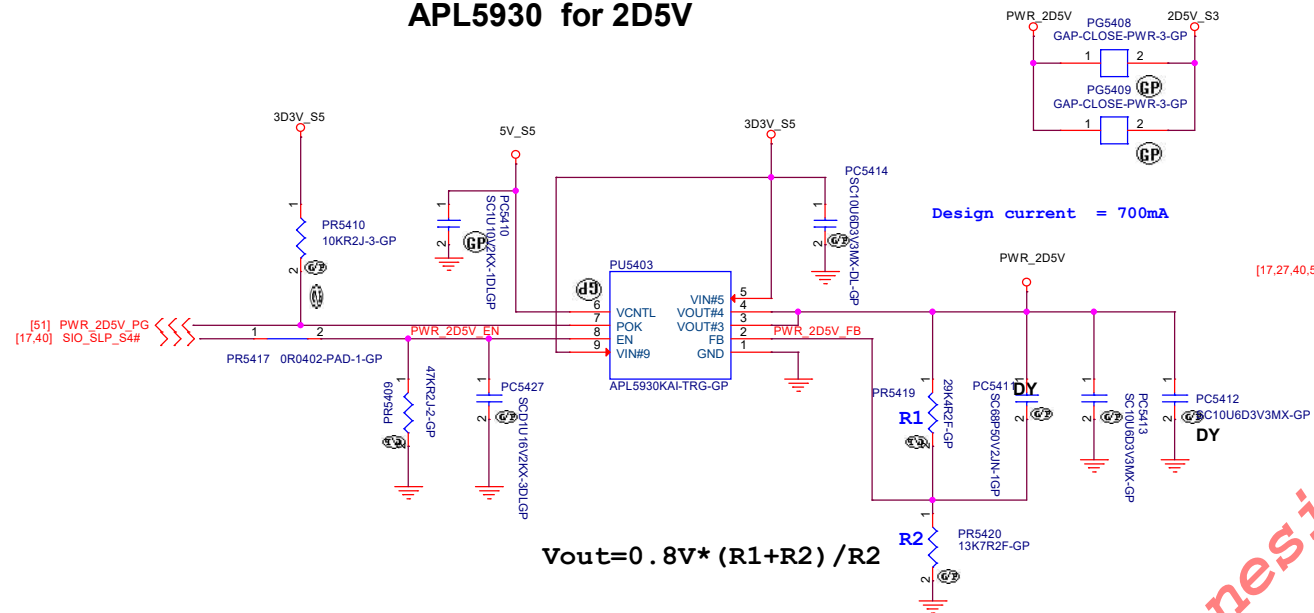
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Size	Document Number	Rev
A3	Starlord KBL-R	A00

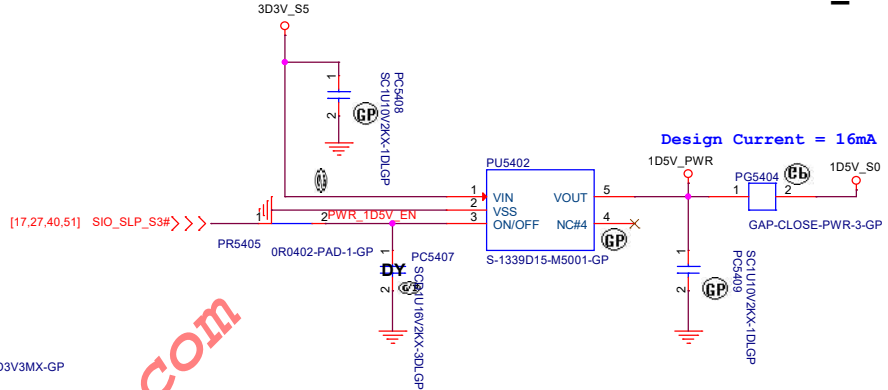
Date: Monday, August 28, 2017	Sheet 53 of 106
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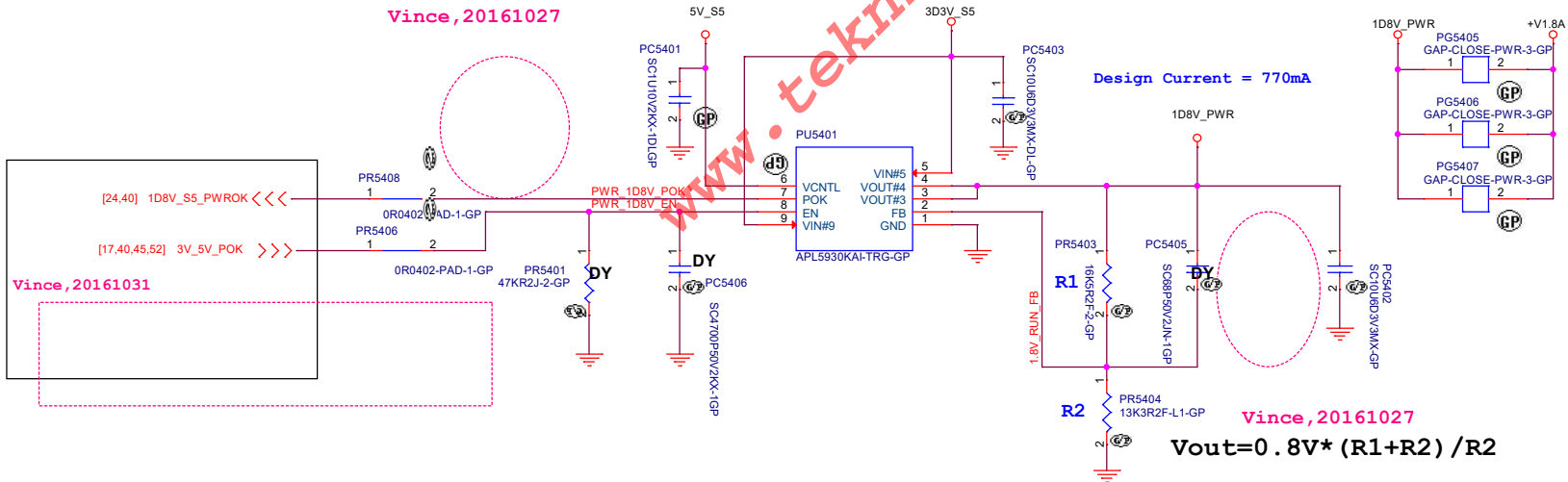
APL5930 for 2D5V



S-1339D15-M5001 for 1D5V_S0



APL5930 for 1D8V_S5



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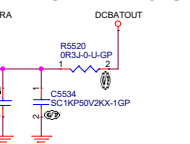
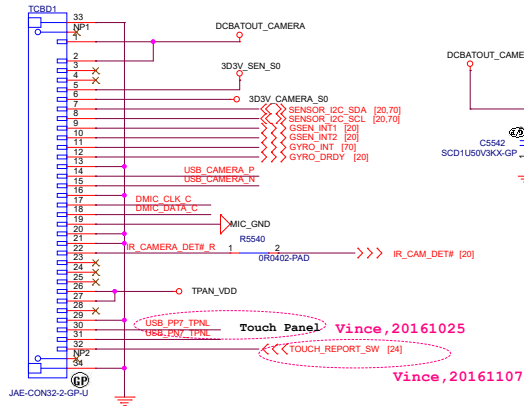
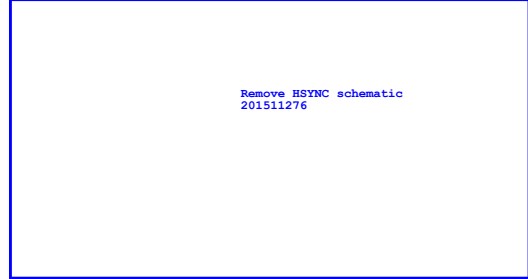
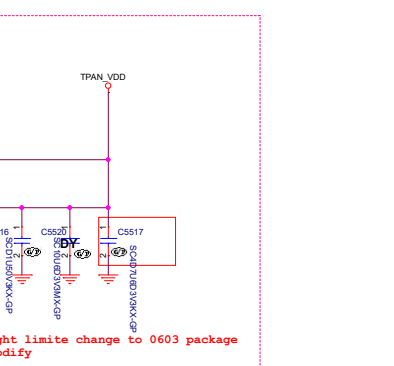
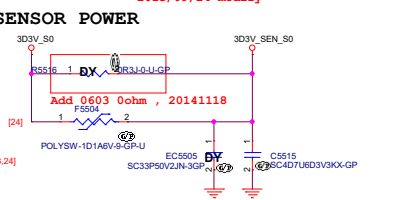
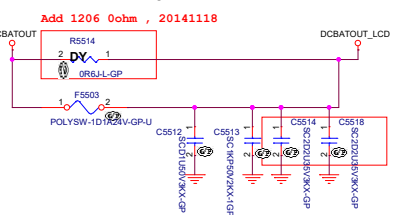
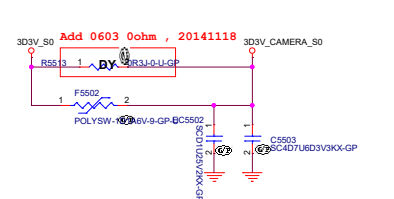
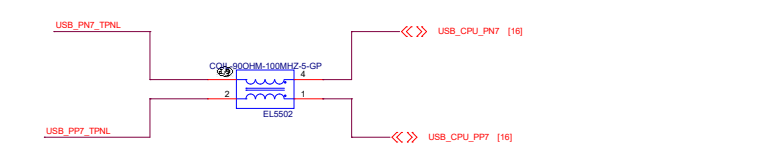
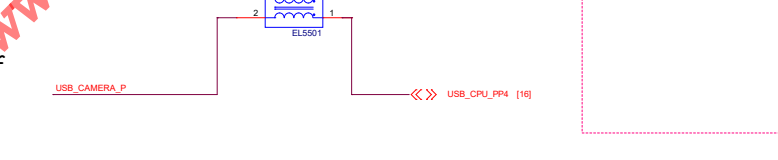
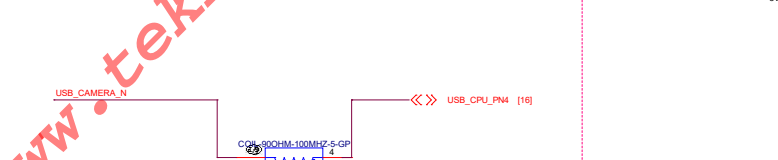
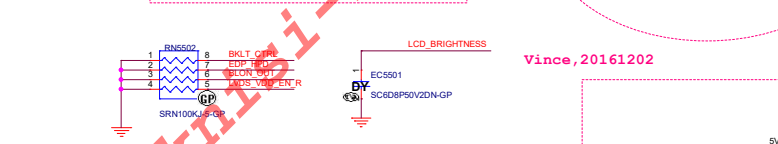
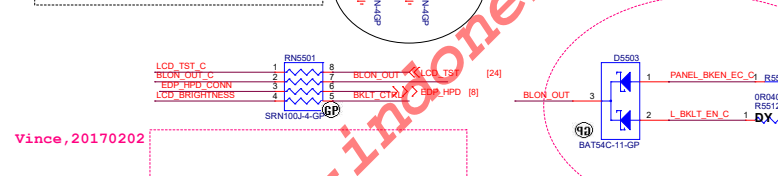
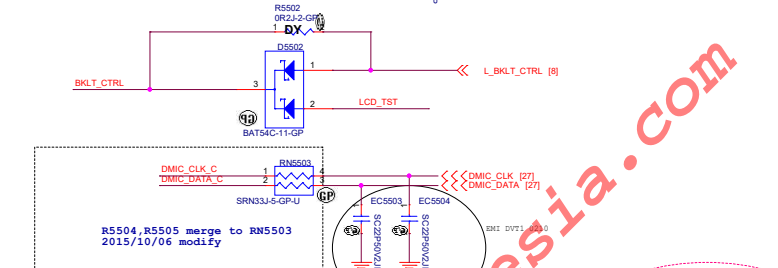
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SSID = LCD



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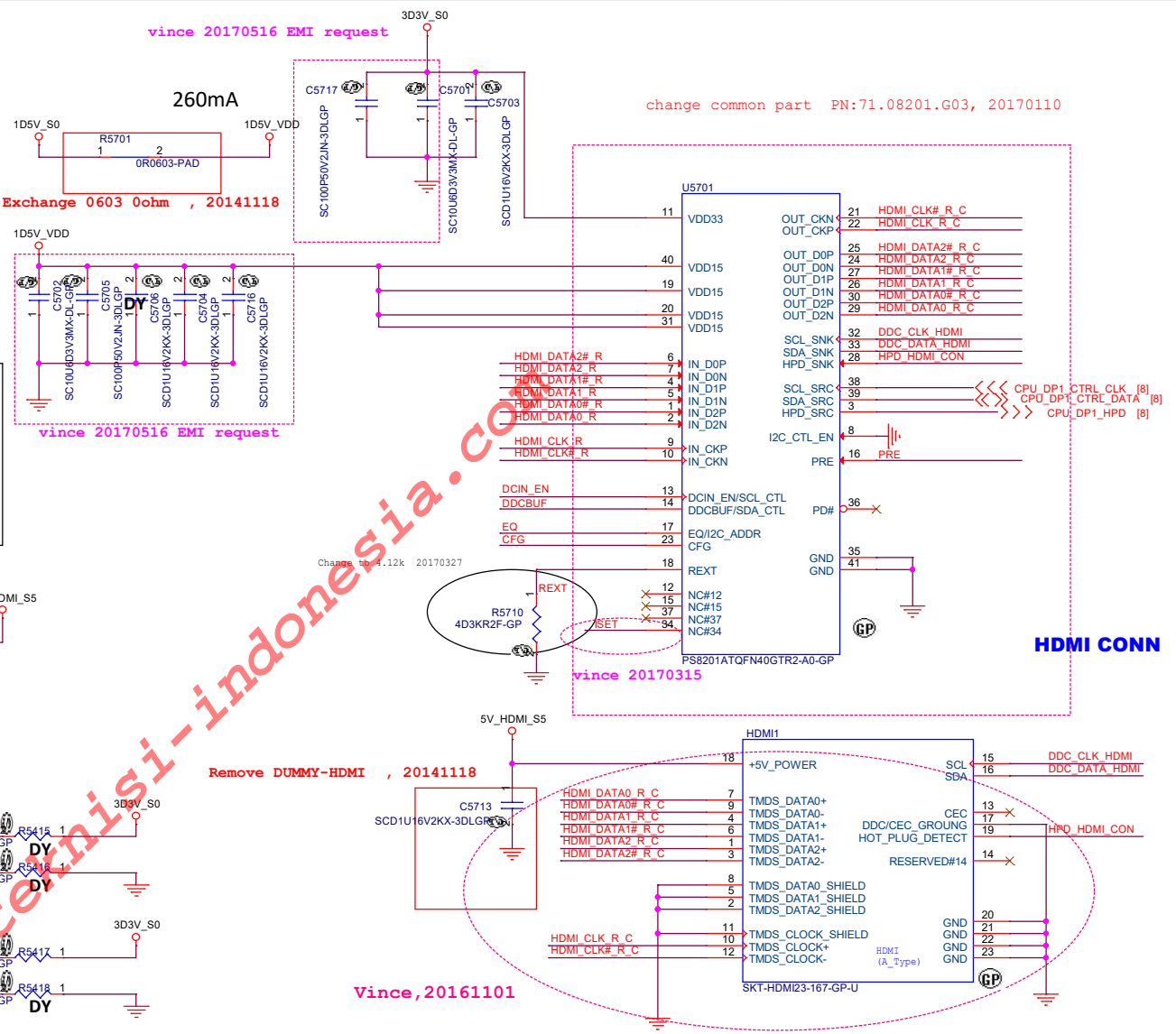
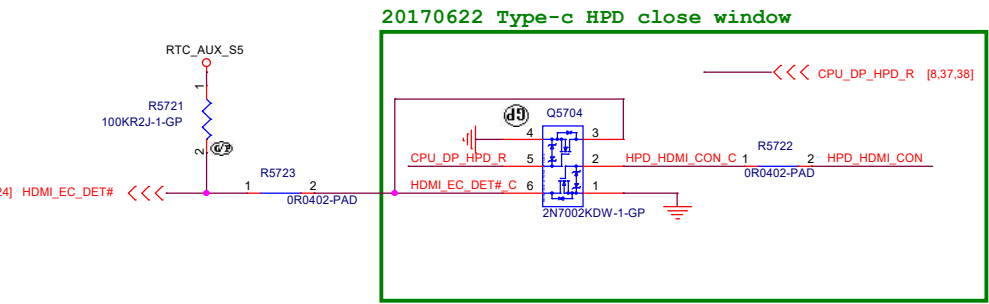
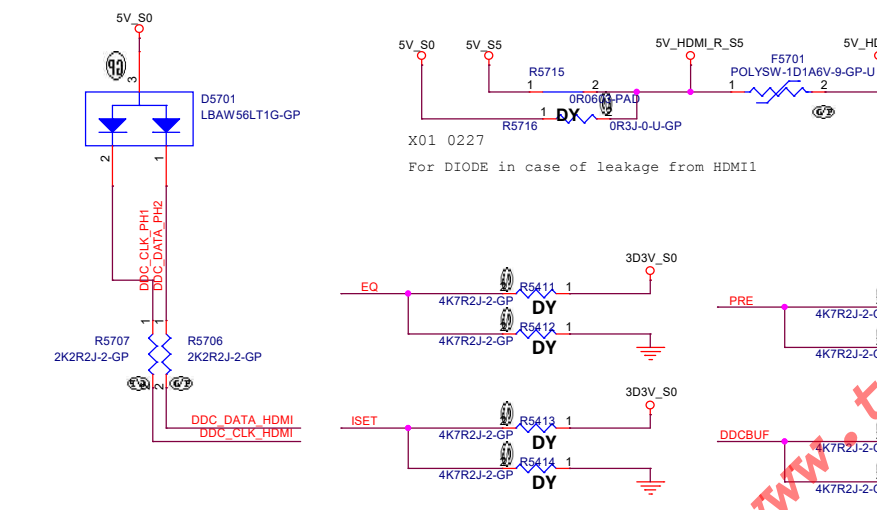
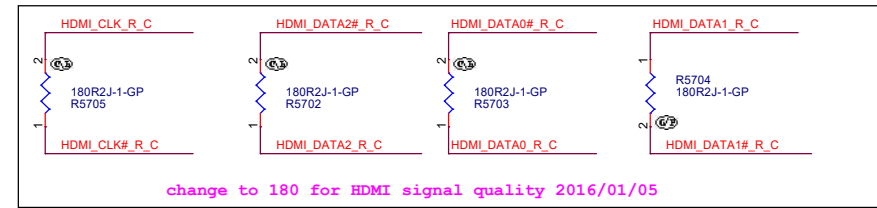
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SSID = HDMI



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Main Func = WLAN

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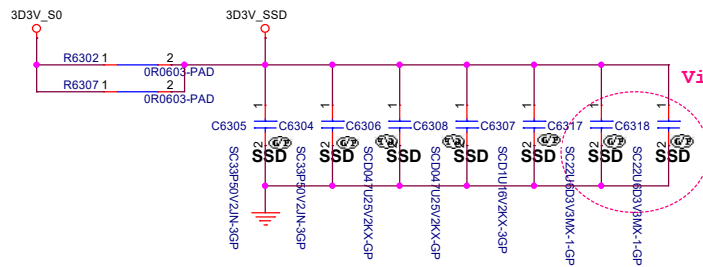
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Reserved			
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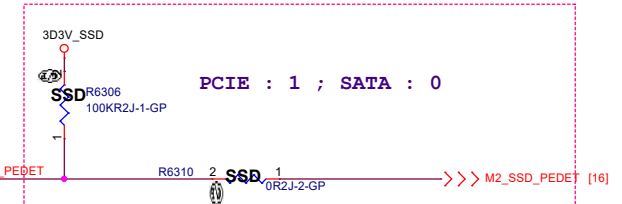
SSD = M.2

Vince, 20160929

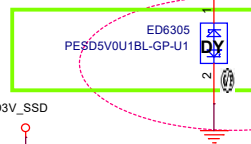


SSD M.2 CONN

Vince, 20161103

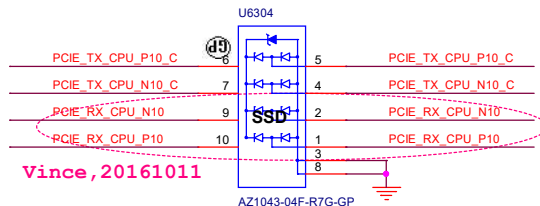
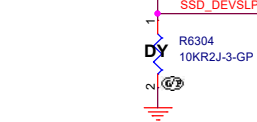


Vince, 20161028



Layout Note:
Need close to SSD1 conn

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.
• This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
• When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.



Vince, 20161011

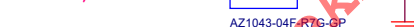


Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

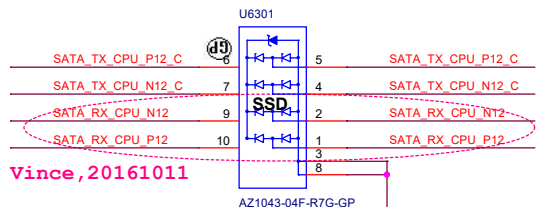
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2 / SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
- Design Constraint: For PCIe* lane that needs to support either PCIe* Gen2 devices or PCIe* Gen3 devices, follow the PCIe* Gen 3 / SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Pin	Signal	Pin	Signal	Pin	Signal
74	3_VAUX	75	3_VAUX	76	3_VAUX
77	3_VAUX	78	3_VAUX	79	3_VAUX
80	3_VAUX	81	3_VAUX	82	3_VAUX
83	3_VAUX	84	3_VAUX	85	3_VAUX
86	3_VAUX	87	3_VAUX	88	3_VAUX
89	3_VAUX	90	3_VAUX	91	3_VAUX
92	3_VAUX	93	3_VAUX	94	3_VAUX
95	3_VAUX	96	3_VAUX	97	3_VAUX
98	3_VAUX	99	3_VAUX	100	3_VAUX
101	3_VAUX	102	3_VAUX	103	3_VAUX
104	3_VAUX	105	3_VAUX	106	3_VAUX
107	3_VAUX	108	3_VAUX	109	3_VAUX
110	3_VAUX	111	3_VAUX	112	3_VAUX
113	3_VAUX	114	3_VAUX	115	3_VAUX
116	3_VAUX	117	3_VAUX	118	3_VAUX
119	3_VAUX	120	3_VAUX	121	3_VAUX
122	3_VAUX	123	3_VAUX	124	3_VAUX
125	3_VAUX	126	3_VAUX	127	3_VAUX
128	3_VAUX	129	3_VAUX	130	3_VAUX
131	3_VAUX	132	3_VAUX	133	3_VAUX
134	3_VAUX	135	3_VAUX	136	3_VAUX
137	3_VAUX	138	3_VAUX	139	3_VAUX
140	3_VAUX	141	3_VAUX	142	3_VAUX
143	3_VAUX	144	3_VAUX	145	3_VAUX
146	3_VAUX	147	3_VAUX	148	3_VAUX
149	3_VAUX	150	3_VAUX	151	3_VAUX
152	3_VAUX	153	3_VAUX	154	3_VAUX
155	3_VAUX	156	3_VAUX	157	3_VAUX
158	3_VAUX	159	3_VAUX	160	3_VAUX
161	3_VAUX	162	3_VAUX	163	3_VAUX
164	3_VAUX	165	3_VAUX	166	3_VAUX
167	3_VAUX	168	3_VAUX	169	3_VAUX
170	3_VAUX	171	3_VAUX	172	3_VAUX
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194	3_VAUX	195	3_VAUX	196	3_VAUX
197	3_VAUX	198	3_VAUX	199	3_VAUX
200	3_VAUX	201	3_VAUX	202	3_VAUX
203	3_VAUX	204	3_VAUX	205	3_VAUX
206	3_VAUX	207	3_VAUX	208	3_VAUX
209	3_VAUX	210	3_VAUX	211	3_VAUX
212	3_VAUX	213	3_VAUX	214	3_VAUX
215	3_VAUX	216	3_VAUX	217	3_VAUX
218	3_VAUX	219	3_VAUX	220	3_VAUX
221	3_VAUX	222	3_VAUX	223	3_VAUX
224	3_VAUX	225	3_VAUX	226	3_VAUX
227	3_VAUX	228	3_VAUX	229	3_VAUX
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287	3_VAUX	288	3_VAUX	289	3_VAUX
290	3_VAUX	291	3_VAUX	292	3_VAUX
293	3_VAUX	294	3_VAUX	295	3_VAUX
296	3_VAUX	297	3_VAUX	298	3_VAUX
299	3_VAUX	300	3_VAUX	301	3_VAUX
302	3_VAUX	303	3_VAUX	304	3_VAUX
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314	3_VAUX	315	3_VAUX	316	3_VAUX
317	3_VAUX	318	3_VAUX	319	3_VAUX
320	3_VAUX	321	3_VAUX	322	3_VAUX
323	3_VAUX	324	3_VAUX	325	3_VAUX
326	3_VAUX	327	3_VAUX	328	3_VAUX
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335	3_VAUX	336	3_VAUX	337	3_VAUX
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386	3_VAUX	387	3_VAUX	388	3_VAUX
389	3_VAUX	390	3_VAUX	391	3_VAUX
392	3_VAUX	393	3_VAUX	394	3_VAUX
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398	3_VAUX	399	3_VAUX	400	3_VAUX



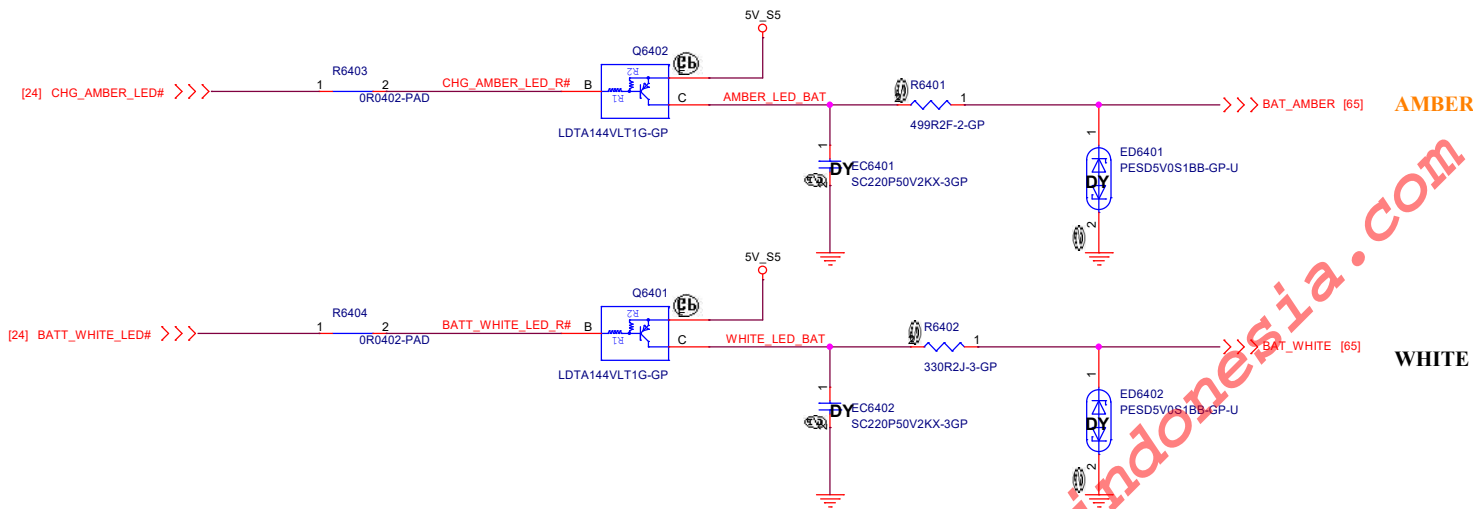
Vince, 20161011

<Core Design>

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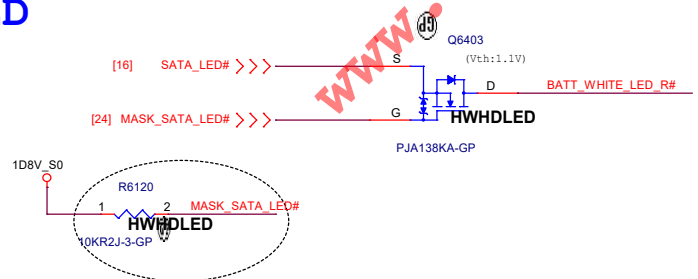
Title (Reserved)		
Size A3	Document Number	Rev
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Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

SATA LED

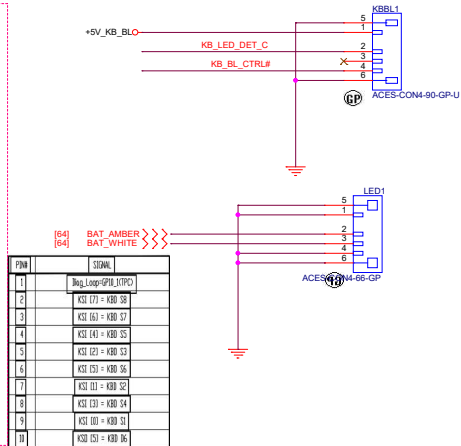
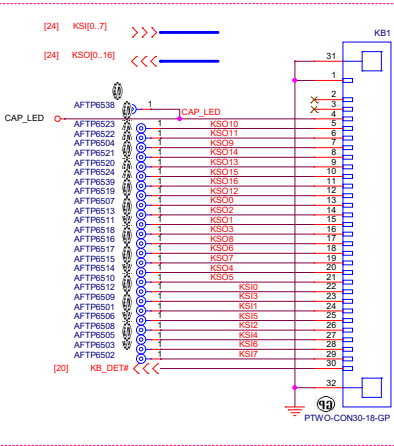


Add SATA LED solution by customer request 2016/02/03

SSID = KB

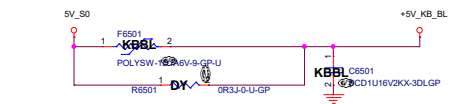
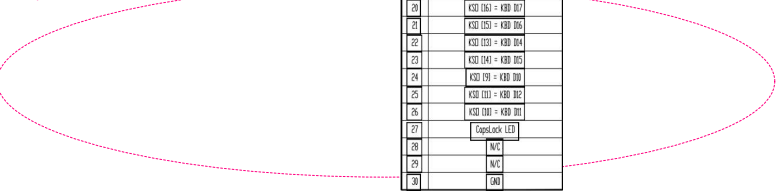
Vince, 20170208

Keyboard

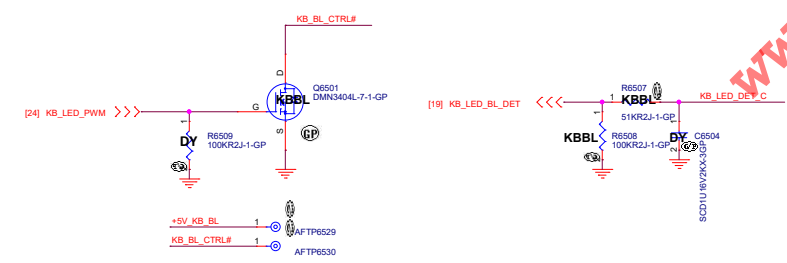


Pin	Signal
1	KB_LED_DET_C
2	KB_LED_CTRL#
3	KB_LED_PWM
4	KB_LED_DET_C
5	KB_LED_CTRL#
6	KB_LED_PWM
7	KB_LED_DET_C
8	KB_LED_CTRL#
9	KB_LED_PWM
10	KB_LED_DET_C
11	KB_LED_CTRL#
12	KB_LED_PWM
13	KB_LED_DET_C
14	KB_LED_CTRL#
15	KB_LED_PWM
16	KB_LED_DET_C
17	KB_LED_CTRL#
18	KB_LED_PWM
19	KB_LED_DET_C
20	KB_LED_CTRL#
21	KB_LED_PWM
22	KB_LED_DET_C
23	KB_LED_CTRL#
24	KB_LED_PWM
25	KB_LED_DET_C
26	KB_LED_CTRL#
27	KB_LED_PWM
28	KB_LED_DET_C
29	KB_LED_CTRL#
30	KB_LED_PWM
31	KB_LED_DET_C
32	KB_LED_CTRL#
33	KB_LED_PWM
34	KB_LED_DET_C
35	KB_LED_CTRL#
36	KB_LED_PWM
37	KB_LED_DET_C
38	KB_LED_CTRL#
39	KB_LED_PWM
40	KB_LED_DET_C
41	KB_LED_CTRL#
42	KB_LED_PWM
43	KB_LED_DET_C
44	KB_LED_CTRL#
45	KB_LED_PWM
46	KB_LED_DET_C
47	KB_LED_CTRL#
48	KB_LED_PWM
49	KB_LED_DET_C
50	KB_LED_CTRL#
51	KB_LED_PWM
52	KB_LED_DET_C
53	KB_LED_CTRL#
54	KB_LED_PWM
55	KB_LED_DET_C
56	KB_LED_CTRL#
57	KB_LED_PWM
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59	KB_LED_CTRL#
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167	KB_LED_CTRL#
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169	KB_LED_DET_C
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189	KB_LED_PWM
190	KB_LED_DET_C
191	KB_LED_CTRL#
192	KB_LED_PWM
193	KB_LED_DET_C
194	KB_LED_CTRL#
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198	KB_LED_PWM
199	KB_LED_DET_C
200	KB_LED_CTRL#

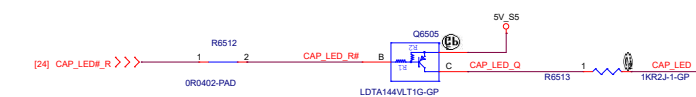
Vince, 20161201



KB Backlight Power Consumption: 285mA max.



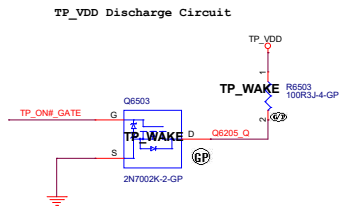
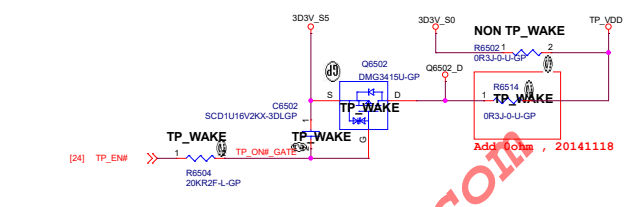
CAP LED Control
LOW acted from KBC GPIO



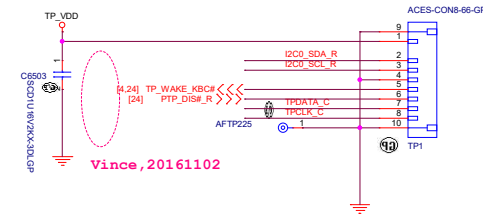
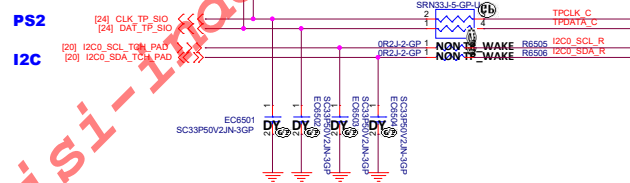
Vince, 20161103



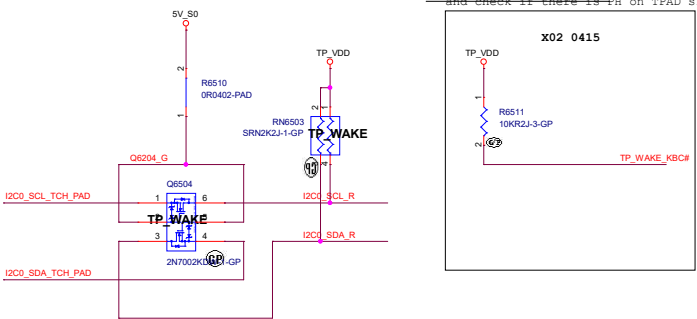
Main Func = TPAD



GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)



Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.



Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)



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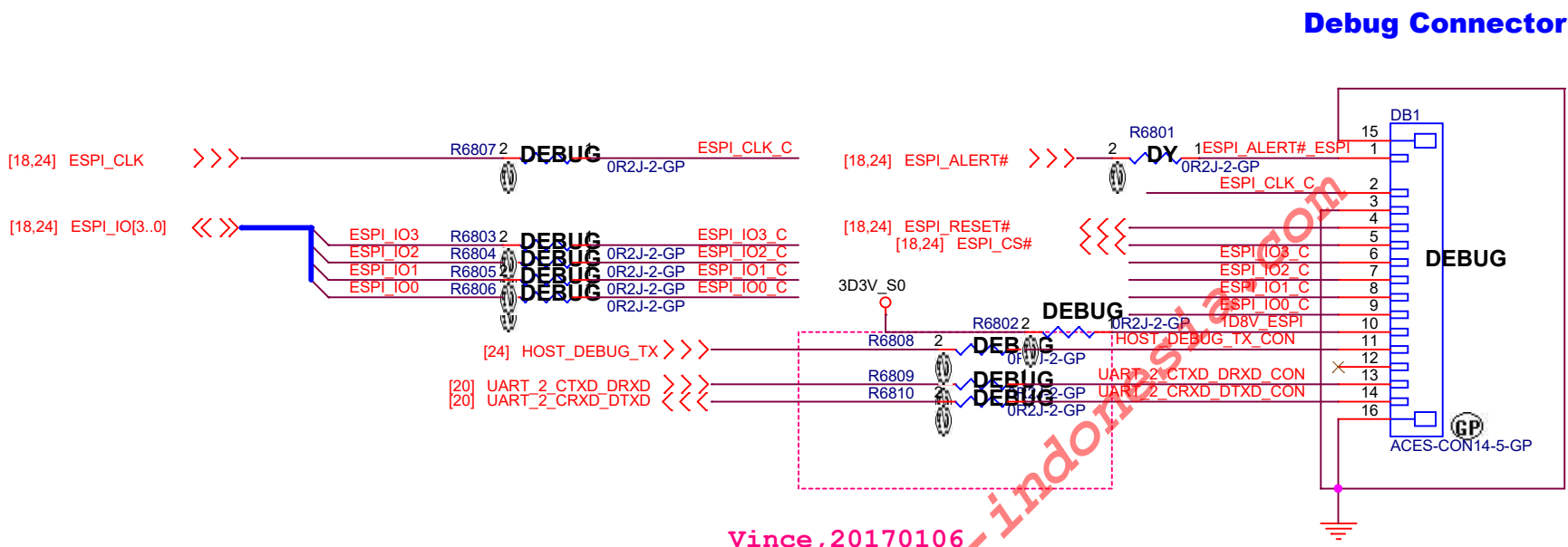
Title

Reserved

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SSID = Debug



Vince,20170106

<Core Design>

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Title Dubug connector			
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Title

Reserved

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Main Func = Hall Sensor

LID sensoe

combine G

Free Fall Sensor + G Sensor

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

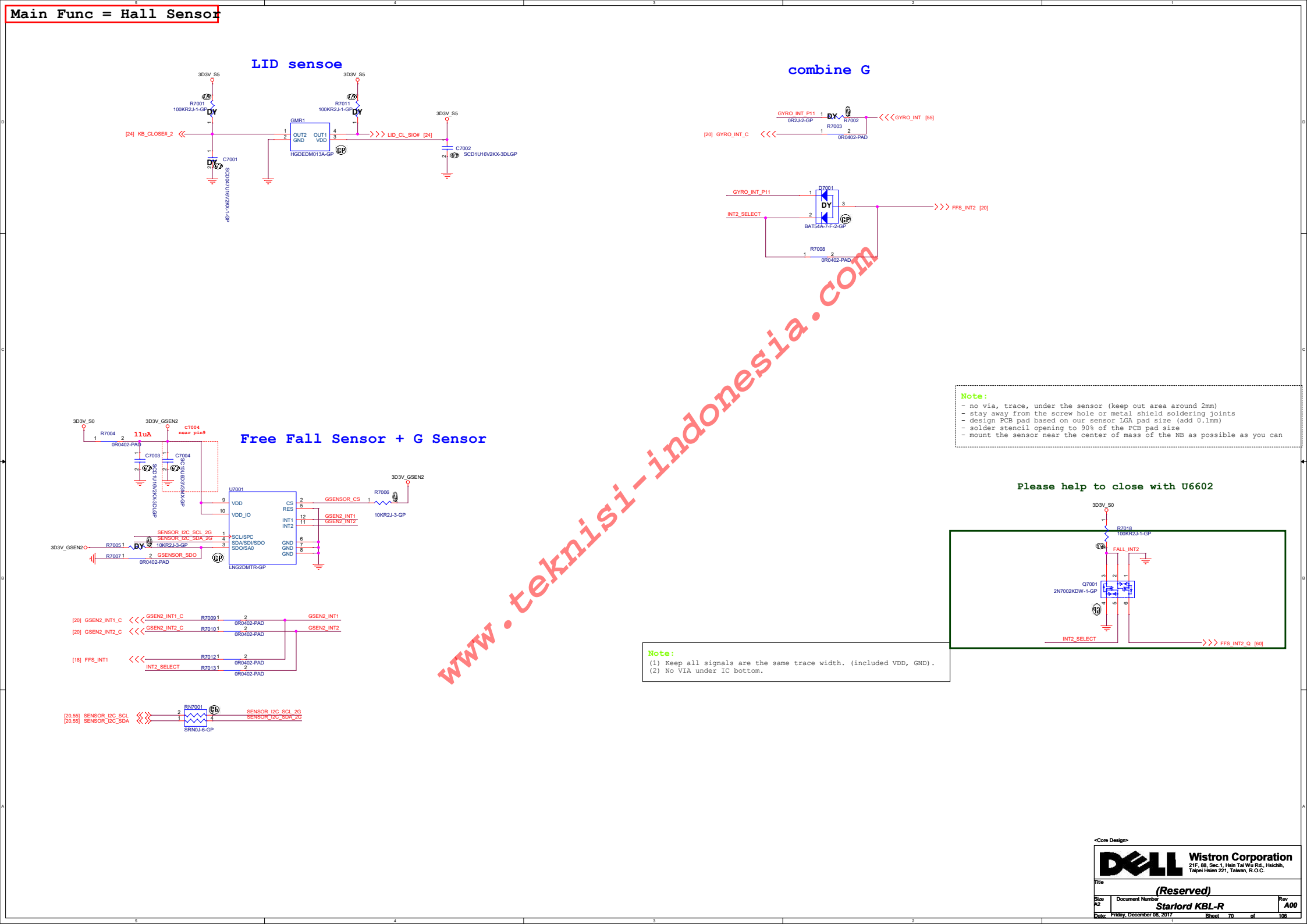
Please help to close with U6602

Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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Main Func = Hall Sensor

LID sensoe

combine G

Free Fall Sensor + G Sensor

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

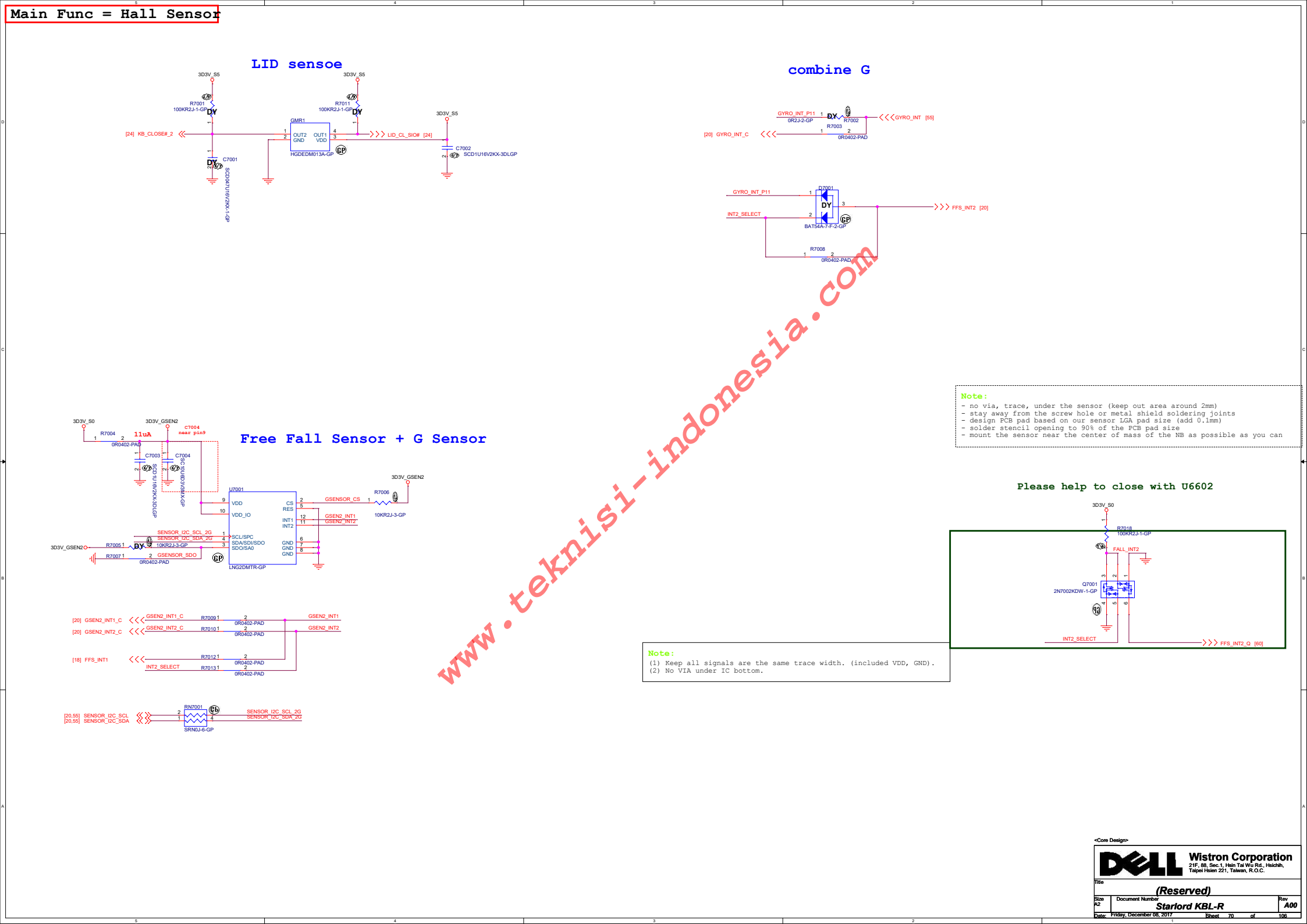
Please help to close with U6602

Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

<Core Design>

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Title	(Reserved)		
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[illegible]

- Main Func = Hall Sensor**

LID sensoe

Schematic diagram for LID sensor. It shows a GMR1 chip connected to 3D3V_S5 and 3D3V_SS. The chip has pins OUT2, GND, OUT1, and VDD. A capacitor C7001 is connected between OUT2 and GND. Resistors R7001 and R7011 are connected between 3D3V_S5 and OUT2. A capacitor C7002 is connected between OUT1 and 3D3V_SS.

combine G

Schematic diagram for combine G sensor. It shows a BAT54A-7-F-2-GP chip connected to GYRO_INT_P11, GYRO_INT_C, INT2_SELECT, and FFS_INT2. The chip has pins 1, 2, 3, and 4. A resistor R7008 is connected between INT2_SELECT and 1. A resistor R7003 is connected between GYRO_INT_C and 2. A resistor R7002 is connected between INT2_SELECT and 3. A resistor R7001 is connected between GYRO_INT_P11 and 4.

Free Fall Sensor + G Sensor

Schematic diagram for Free Fall Sensor + G Sensor. It shows a U7001 chip connected to 3D3V_GSEN2, 3D3V_GSENZ, and 3D3V_S5. The chip has pins VDD, CS, RES, INT1, INT2, GND, and SDO. A capacitor C7004 is connected between VDD and CS. A capacitor C7003 is connected between CS and RES. A resistor R7004 is connected between 3D3V_S5 and CS. A resistor R7007 is connected between 3D3V_GSEN2 and INT1. A resistor R7008 is connected between 3D3V_GSENZ and INT2. A resistor R7009 is connected between INT1 and GND. A resistor R7010 is connected between INT2 and GND. A resistor R7012 is connected between INT1 and GND. A resistor R7013 is connected between INT2 and GND. A resistor R7001 is connected between INT1 and GND. A resistor SRN015-GP is connected between INT2 and GND.

Note:

 - no via, trace, under the sensor (keep out area around 2mm)
 - stay away from the screw hole or metal shield soldering joints
 - design PCB pad based on our sensor LGA pad size (add 0.1mm)
 - solder stencil opening to 90% of the PCB pad size
 - mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602

Main Func = Hall Sensor

LID sensoe

combine G

Free Fall Sensor + G Sensor

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

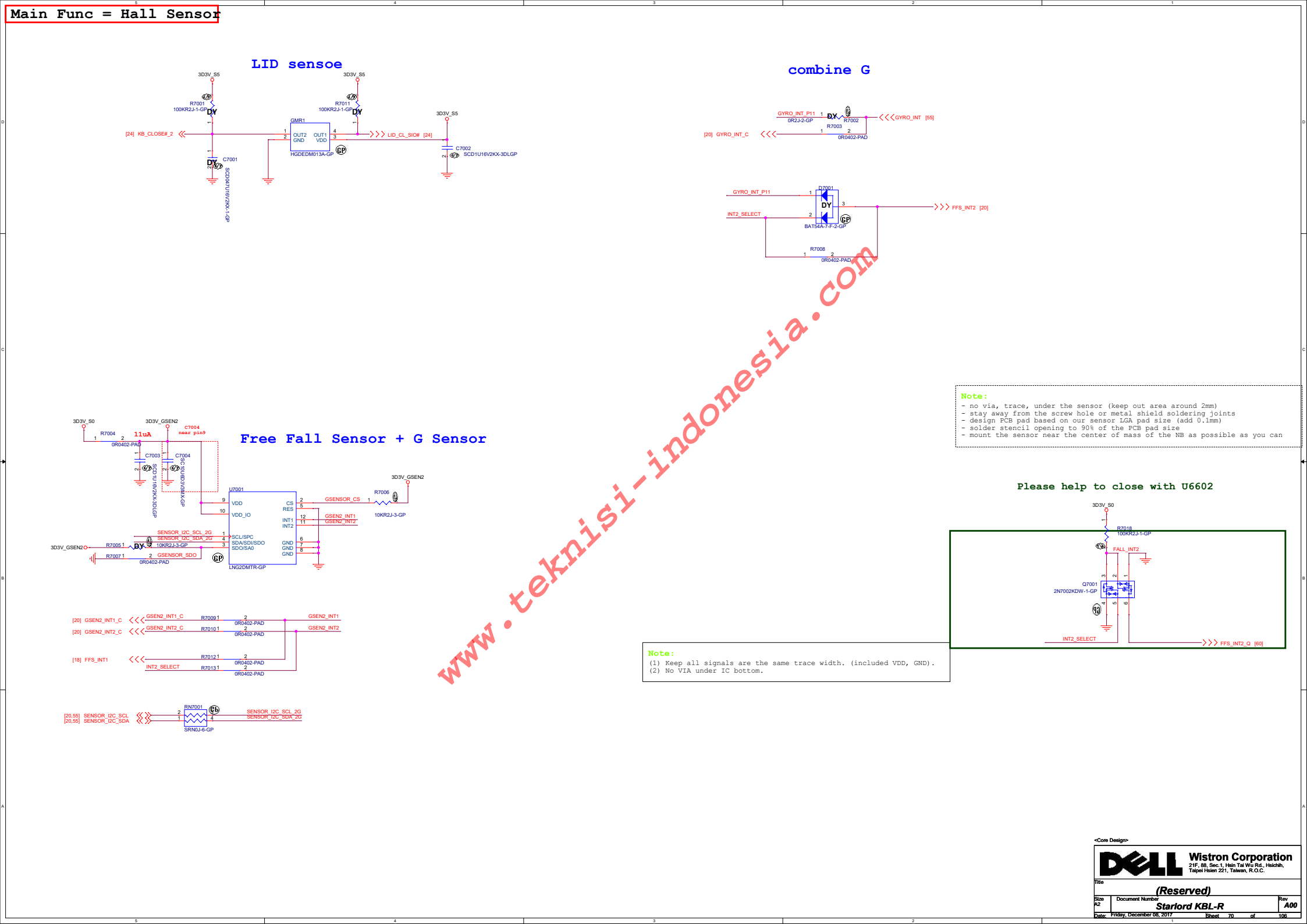
Please help to close with U6602

Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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Main Func = Hall Sensor

LID sensoe

Schematic diagram for LID sensor. It shows a GMR1 chip connected to a 3D3V_S5 supply. The chip has pins OUT2, GND, OUT1, and VDD. Connections include R7001, R7011, C7001, and C7002. A signal trace [24] KB_CLOSE#_2 is shown.

combine G

Schematic diagram for combine G sensor. It shows a connection between GYRO_INT_P11 and GYRO_INT_C. The signal is processed by a component labeled BAT54A-7-F-2-GP. The output is FFS_INT2 [20].

Free Fall Sensor + G Sensor

Schematic diagram for Free Fall Sensor + G Sensor. It features a U7001 chip connected to a 3D3V_GSEN2 supply. The chip has pins VDD, CS, RES, INT1, INT2, SCL/SPC, SDA/SDI/SDO, and SDO/SAO. Connections include R7004, C7004, R7008, and various sensors like SENSOR_I2C_SCL_2G, SENSOR_I2C_SDA_2G, and SENSOR_I2C_SDO. Signal traces for GSEnz_INT1_C, GSEnz_INT2_C, FFS_INT1, and INT2_SELECT are shown.

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602

Schematic diagram for U6602. It shows a connection between Q7001 and R7018. The signal is processed by a component labeled FALL_INT2. The output is FFS_INT2_Q [60].

Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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- Main Func = Hall Sensor**

LID sensoe

combine G

Free Fall Sensor + G Sensor

Please help to close with U6602

Note:

 - no via, trace, under the sensor (keep out area around 2mm)
 - stay away from the screw hole or metal shield soldering joints
 - design PCB pad based on our sensor LGA pad size (add 0.1mm)
 - solder stencil opening to 90% of the PCB pad size
 - mount the sensor near the center of mass of the NB as possible as you can

Note:

 - (1) Keep all signals are the same trace width. (included VDD, GND).
 - (2) No VIA under IC bottom.

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Main Func = Hall Sensor

LID sensoe

combine G

Free Fall Sensor + G Sensor

Please help to close with U6602

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

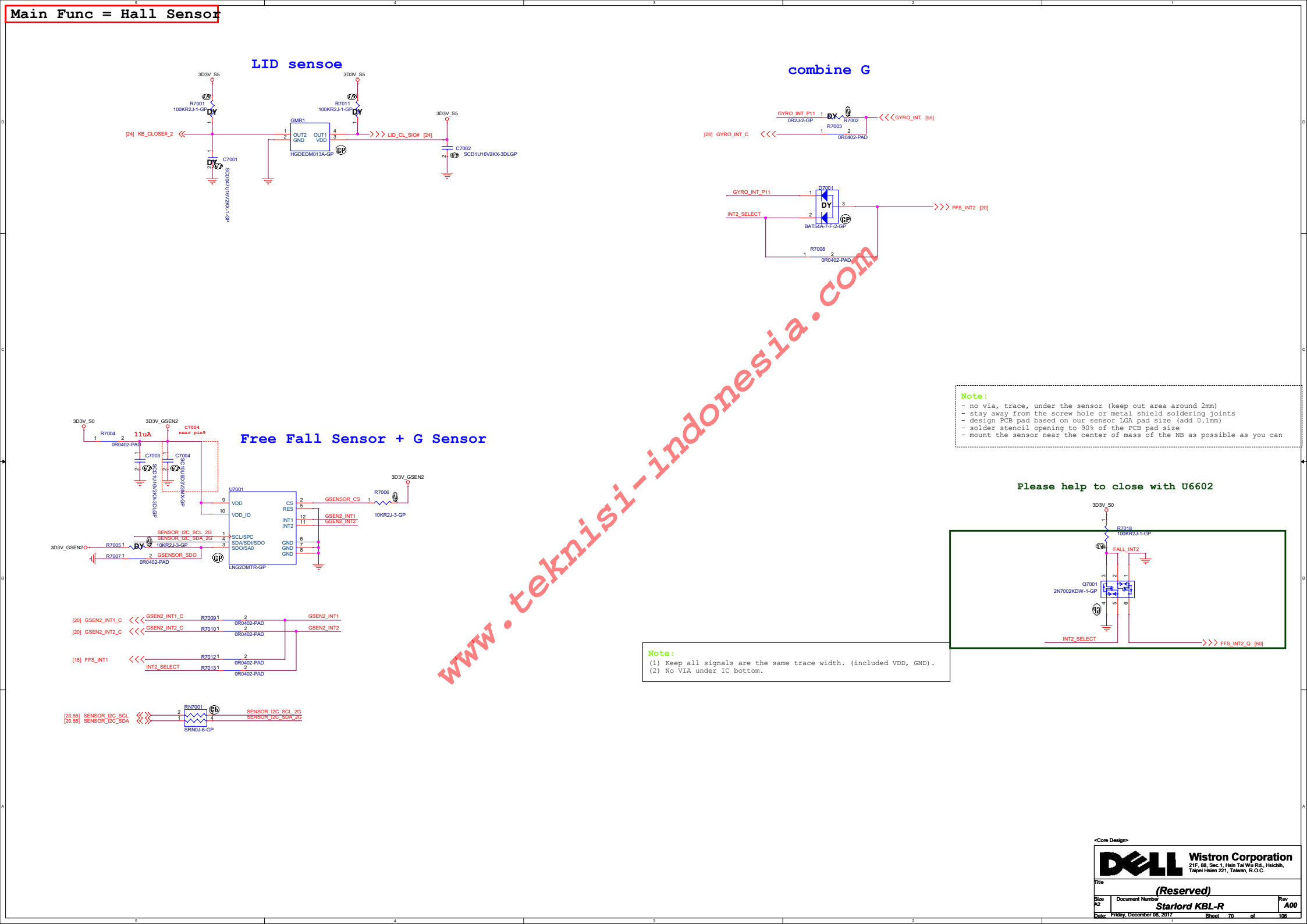
Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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Title

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Title

USB3.0 PORT

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Title GPU(2/5)DIGITALOUT			
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Main Func = dGPU

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Title

GPU(5/5)PWR/GND

Size

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Custom

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Main Func = dGPU

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Title

GPU-VRAM1,2 (1/4)

Size

A3

Document Number

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Main Func = dGPU

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Title

GPU-VRAM3,4 (2/4)

Size
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Main Func = dGPU

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Main Func = dGPU

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Main Func = dGFX_CORE

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GPU CORE					
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Main Func = dGPU

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GPU Discrete Power					
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Title

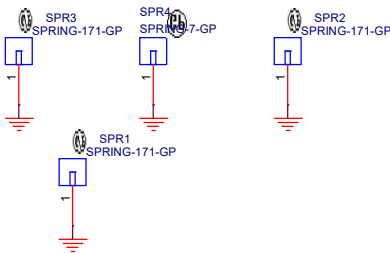
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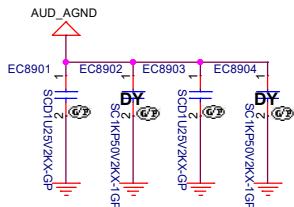
SSID = UnusedParts

34.4YW18.001

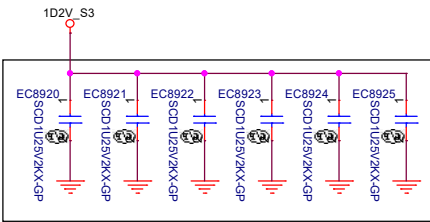


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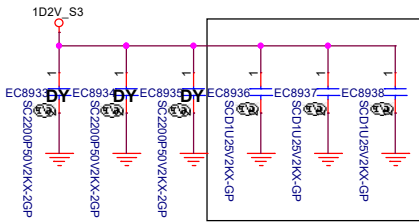
Mind the voltage rating of the caps.



SSID = RF

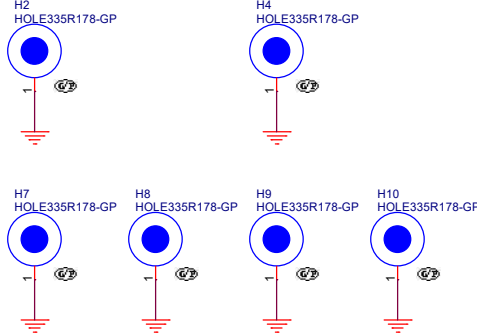


Change to 0.1uF at 20150427 for EMI

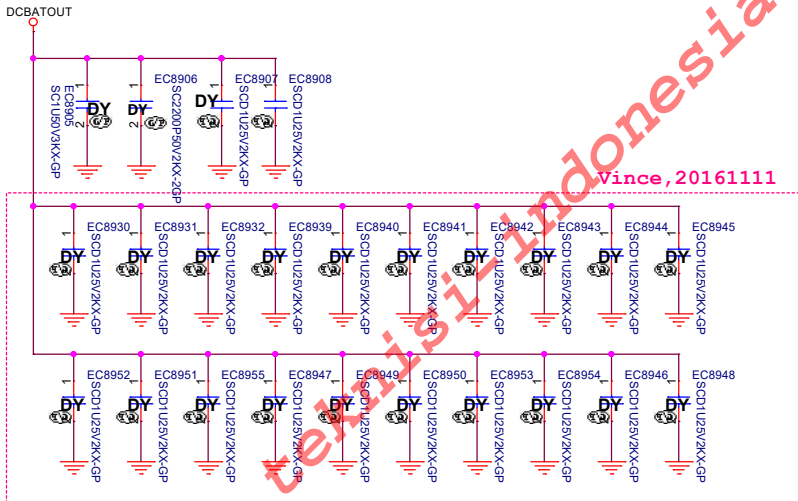
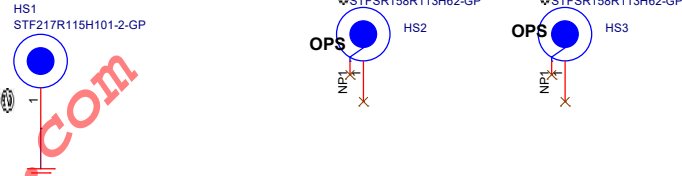
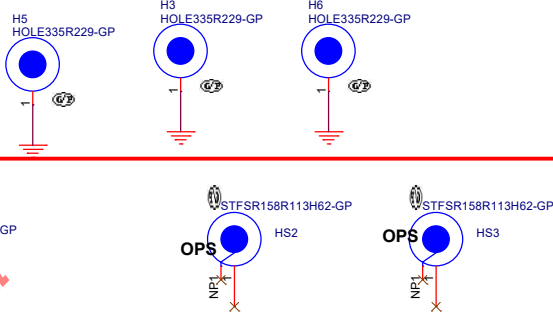


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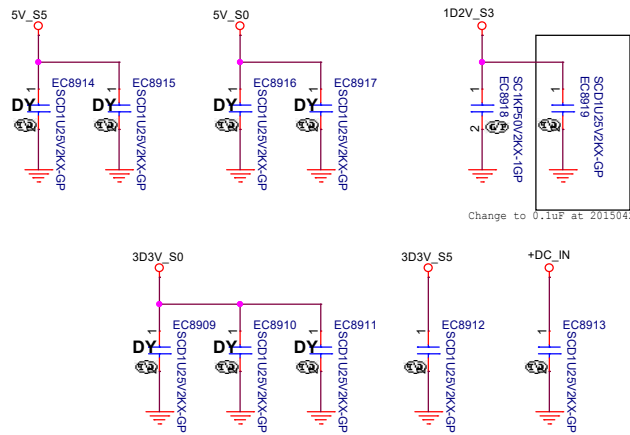
ZZ.00PAD.7F1



ZZ.00PAD.7G1



Remove EC8931,EC8932,EC8926,EC8930for placement



Change to 0.1uF at 20150427 for EMI



RF request 2016/01/12 modify

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LVDS Switch

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Title

CRT Switch

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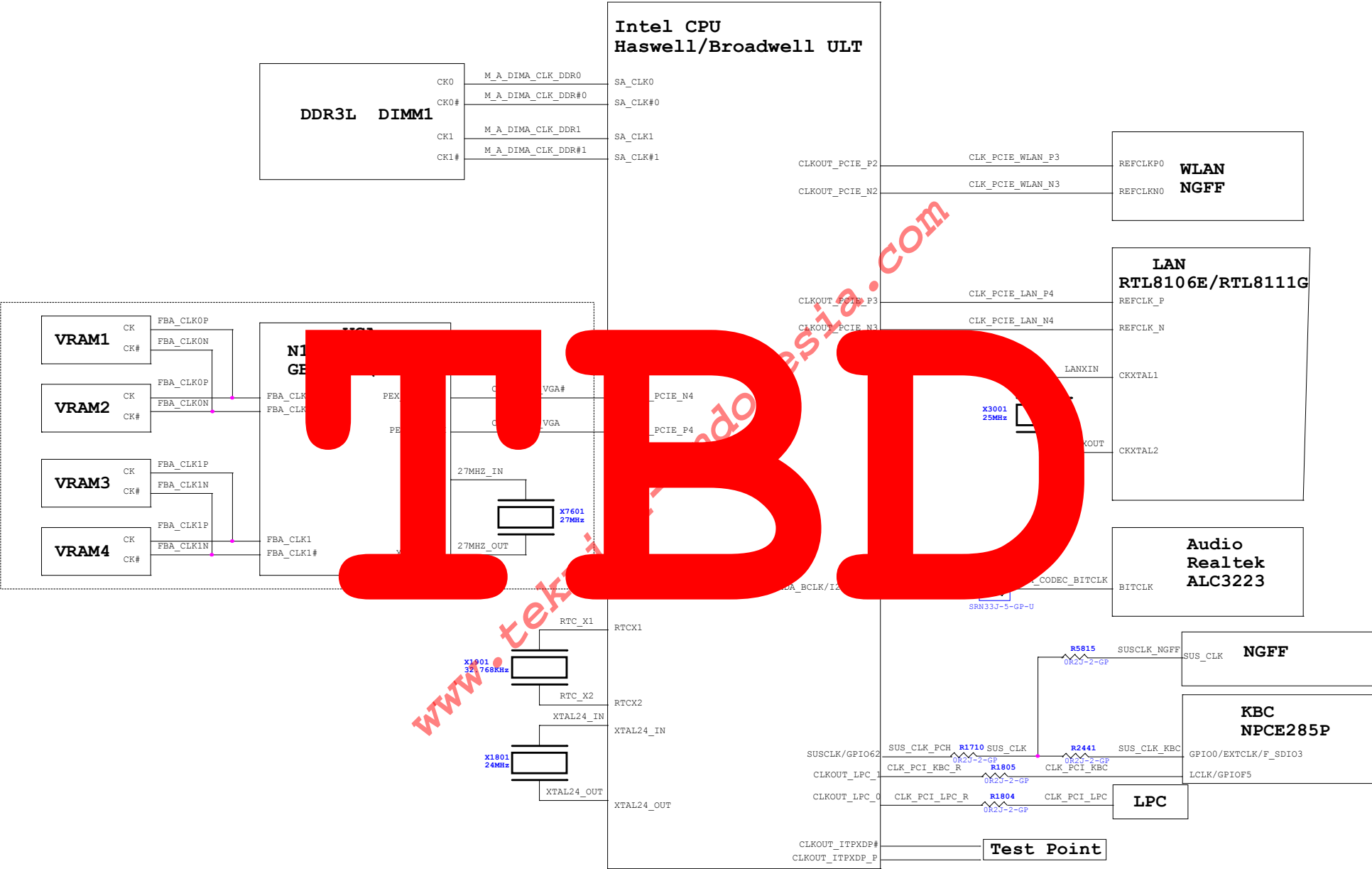
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```
Main Func = Debug
```

CLK Block Diagram



[illegible]

DELL

Change History

Starlord KBL-R

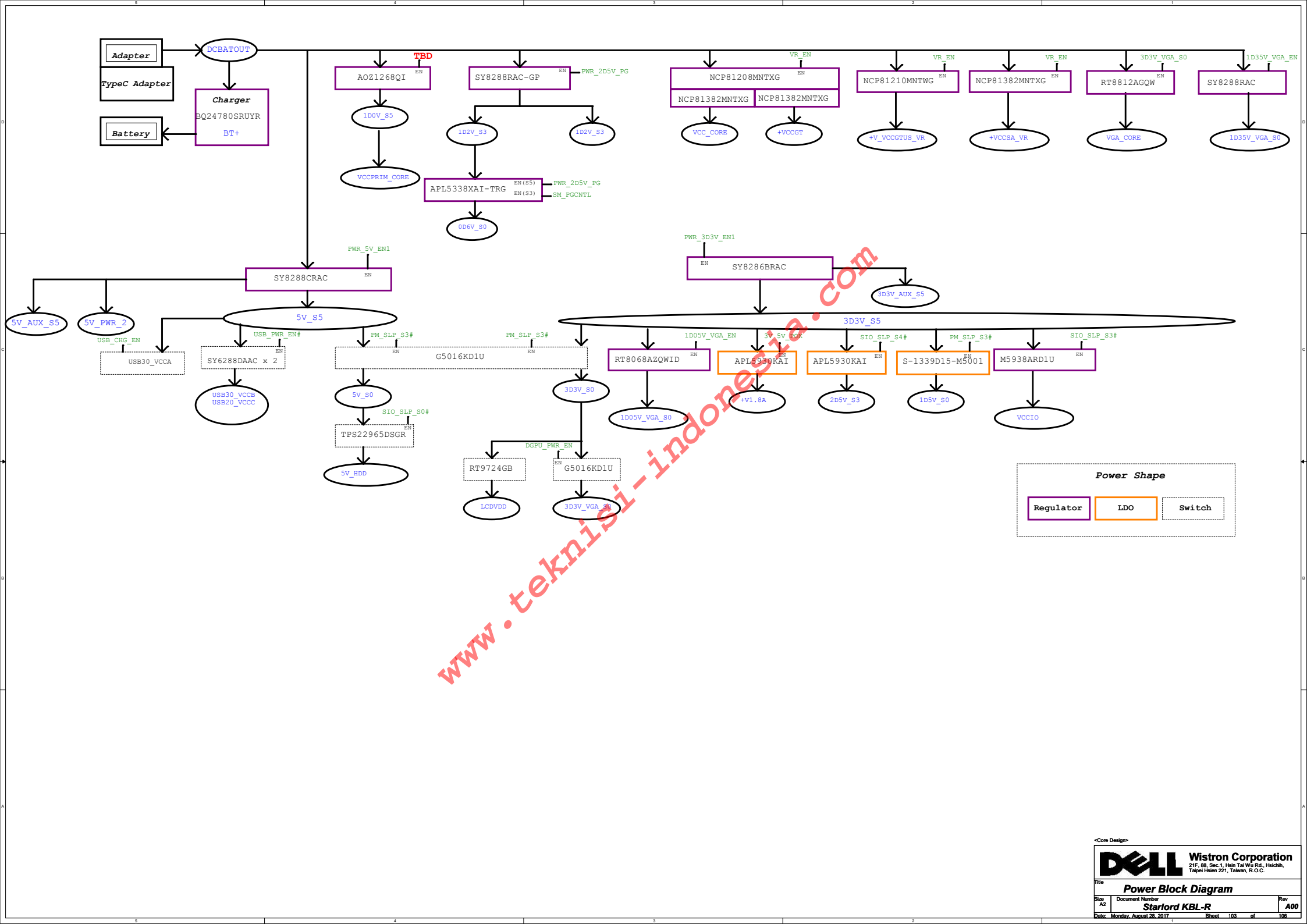
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There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

- ALL Rail PG0DDn1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6s for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

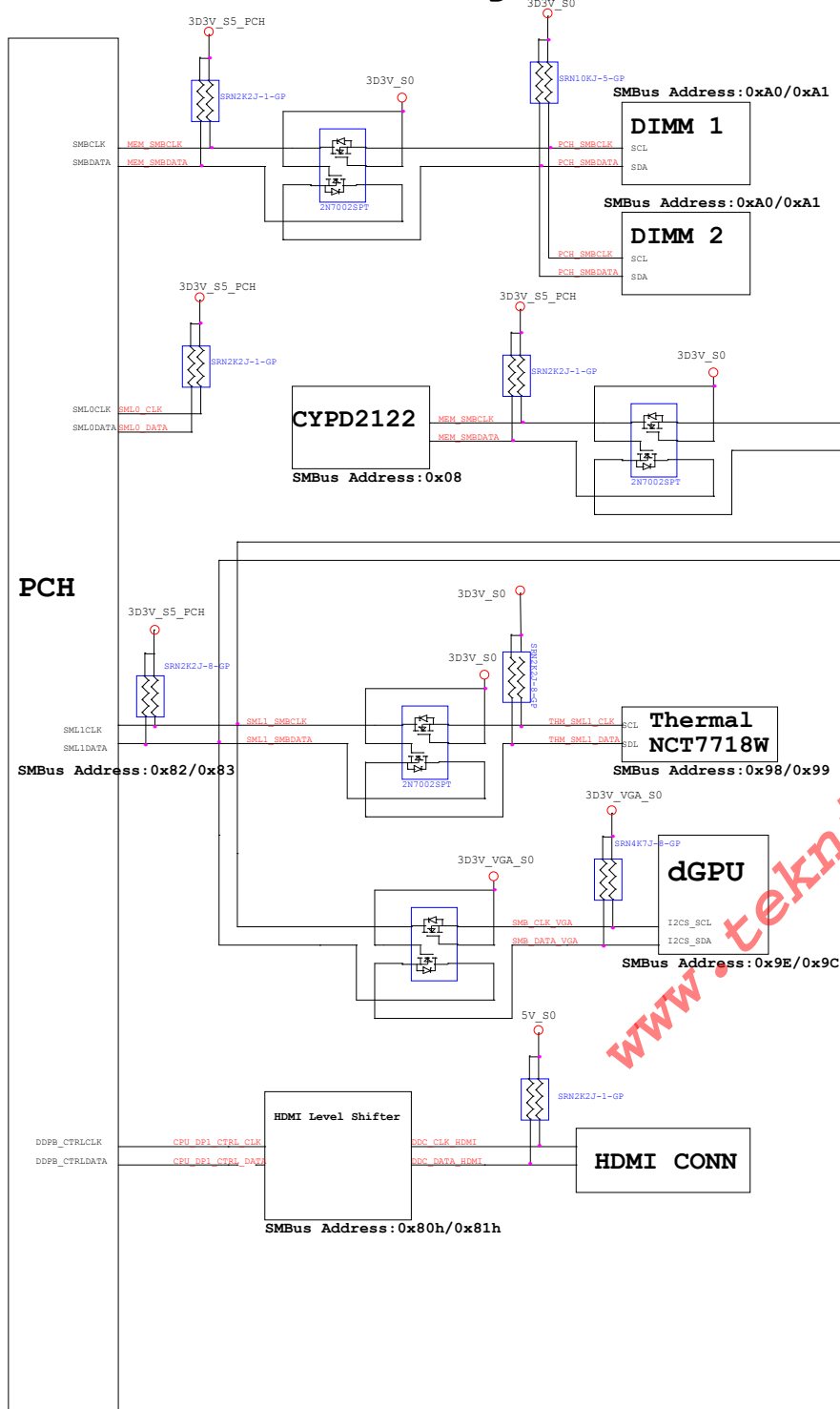
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Power Sequence		
Standard KRL-R		

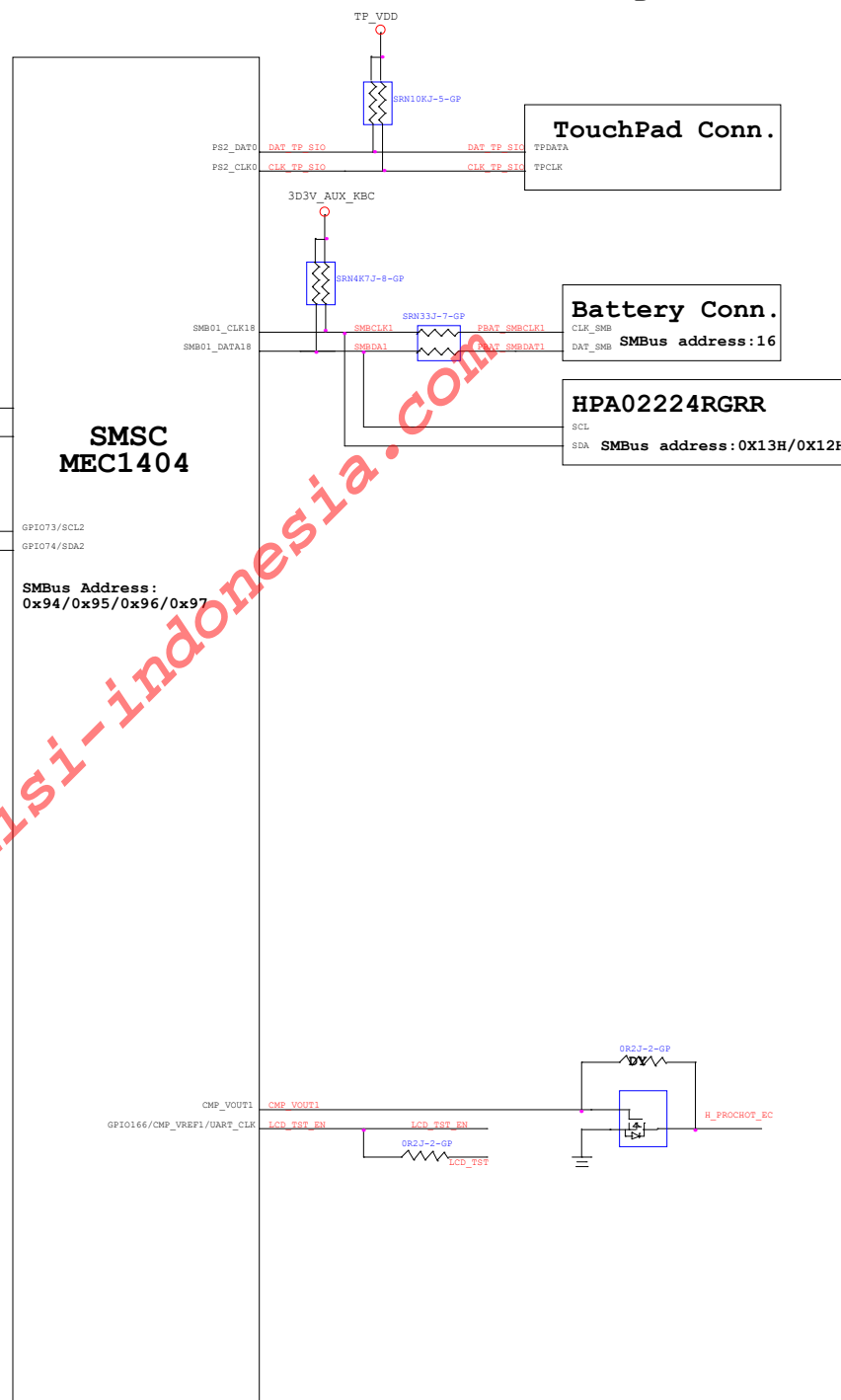


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PCH SMBus Block Diagram

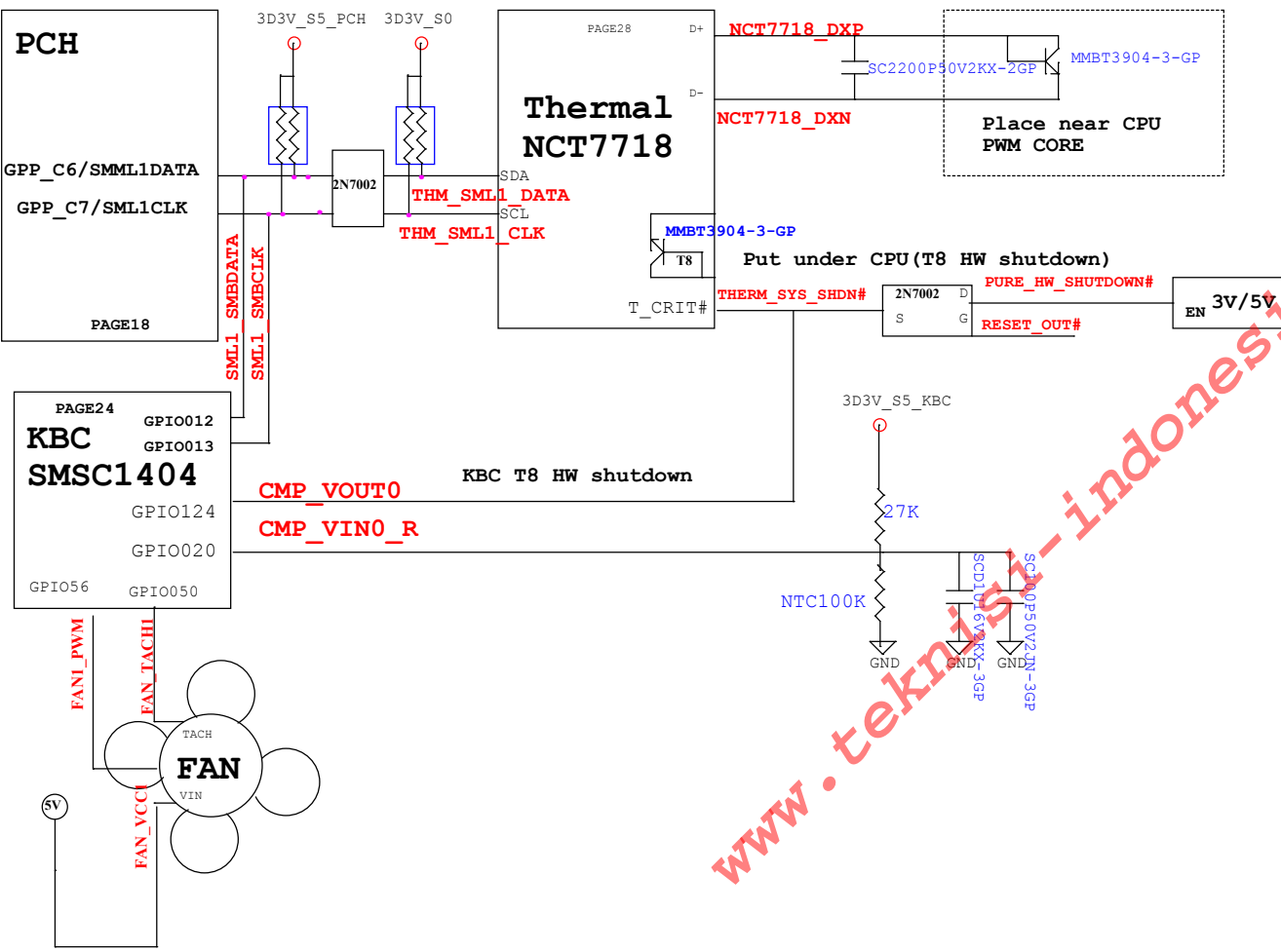


KBC SMBus Block Diagram

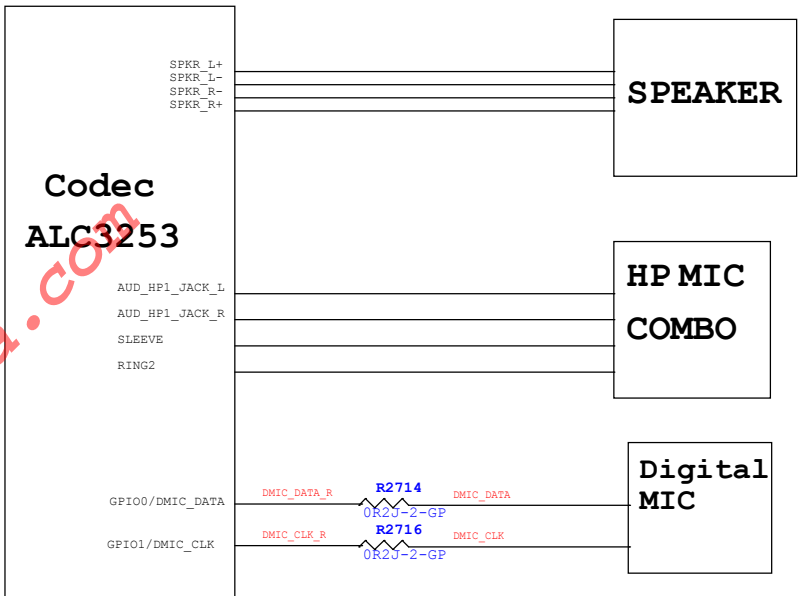


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Thermal Block Diagram



Audio Block Diagram



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SIP connector

Size
A

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